AEROFLEX GAISLER

GR712 Development Board

User Manual

AEROFLEX GAISLER AB

Rev. 0.11, 2014-08-08

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REVISION HISTORY

Revision	Date	Page	Description
0.1	2011-01-24		New document
0.2	2011-02-03	§2.13 §4.2 §3	Changed 'DSU-BREAK" switch to 'not used' Updated figures
0.3	2011-02-24	-	Various small edits
0.4	2011-03-29	30	Corrected GRMON command
0.5	2011-07-22	§2.6.2	Added additional text to describe setting SpW Clock Divisor Registers
0.6	2011-10-03	§2.13 Table 4-1 Table 4-15	Added mention of FT2232 chip for USB-JTAG Interface Corrected JTAG connector type for J12 / Mini-USB Corrected pin names for J12 / Mini-USB
0.7 0.7a	2012-02-22 2012-02-23	§2.3.3 §2.12, Table 4-36 Table 3-1	Added note about maximum SDRAM clock speed Corrected references to jumper JP1 and its pinning. Correct defaults for JP1, JP2.
0.8	2013-01-21	§3	Removed '-i' option as not compatible with latest versions of grmon/grmon2.
0.9	2013-08-28	RD-5 & §2.3.4	Added reference document and information on expansion connector pin numbering Added clarification for jumper numbering/lettering
0.10	2013-10-23	Figure 2-6 Table 3-1 & 4-33	Corrected Jumper position labels for expansion connector pin numbering Correct typo: Default frequency is 48MHz.
0.11	2014-08-08	§1.3 Table 3-1	Removed spurious third paragraph Changed 'default' status of JP88 to 'not installed' since a separate 100MHz oscillator (X5) is installed for SPW_CLK Changed default state of JP84 to 2-3 to use 80MHz oscillator in X2.

1 INTRODUCTION

1.1 Overview

This document describes the *GR712 Development Board.*

The purpose of this equipment is to provide developers with a convenient hardware platform for the evaluation and development of software for the *Aeroflex Gaisler GR712RC Dual Core Leon3FT SparcV8 Processor.* The *GR712RC* is a *LEON3FT Fault-Tolerant architecture* custom ASIC for Aerospace applications.

The *GR712-BOARD* comprises a custom designed PCB in a Double Eurocard format (233.5 x 160mm) making the board suitable for stand-alone bench top development, or suitable for mounting in a housing. The principle interfaces and functions are accessible on the front and back edges of the board.

The *GR712RC* chip incorporates an internal programmable switch matrix which means that the same input/output pin can be used for multiple functions. This board therefore has a large number of configuration features in order to be able to exercise and configure the functions of the device.

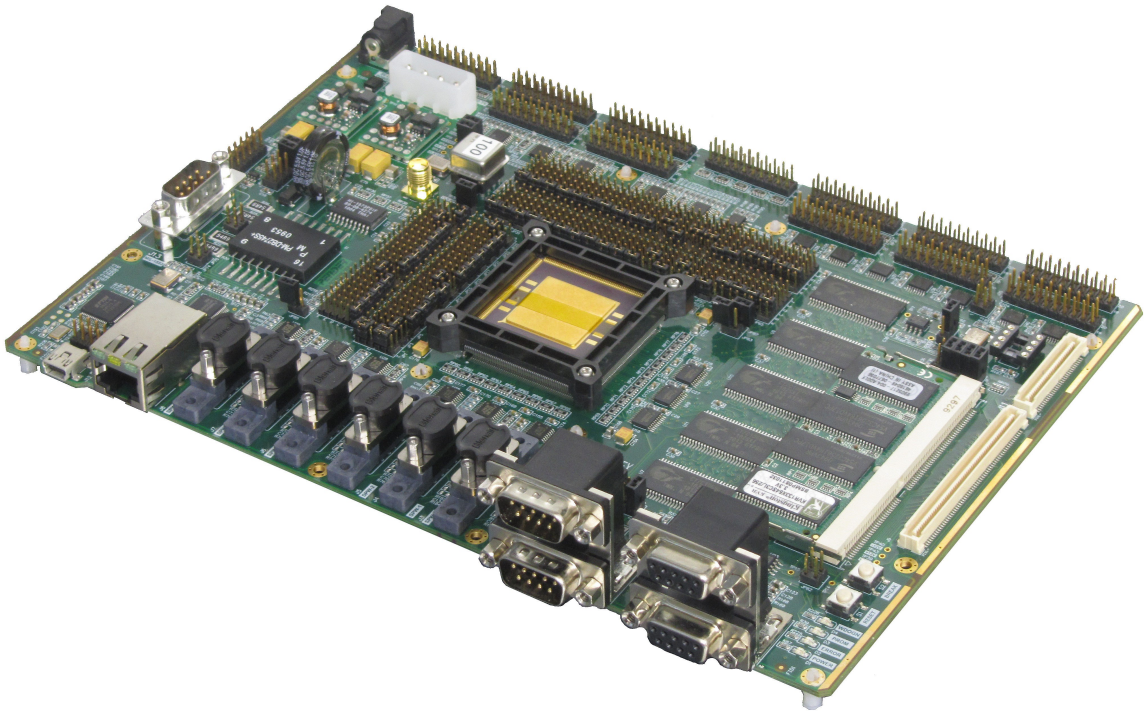

Figure 1-1: GR712 Development Board

The PCB contains the following main items as detailed in section 2 of this document:

- GR712RC ASIC
- Memory
  - SRAM 80 Mbit (1 bank x 2Mword x 40 bit, typ. 10ns) (optional second bank is not fitted as standard)
  - SDRAM SODIMM socket (up to 64Mword x 48 bit with 512Mbyte module)
  - FLASH 64Mbit (8M x 8 bit, typ. 90ns)
  - additional memory options possible via memory expansion connector
- Power, Reset, Clock and Auxiliary circuits
- Interface circuits required for the features listed below

The interface connectors on the Front edge of the board provide:

- Two Serial UART interface (RS232) with D9 Sub female connectors
- Ethernet, 10/100Mbit RMII interface with RJ45 jack
- JTAG – DSU interface
- Two CAN bus interfaces (ISO 11898) with D9 Sub male connectors
- Two dedicated Spacewire interfaces (MDM9S connectors)
- Four optional Spacewire interfaces (MDM9S connectors)

To enable convenient connection to the interfaces, the connector types and pin-outs are compatible with the standard connector types for these types of interfaces.

The interface connectors on the Back edge of the board provide:

- +5V input power connector
- 64 pins General Purpose I/O Port on 0.1” headers (some shared with other functions)
- 20 RS422 Transmit pairs, on 0.1” headers
- 28 RS422 Receive pairs, on 0.1” headers

Additionally, on-board headers and components provide access to the following functions/ features:

- Dual MIL-STD-1553B communication interface
- I2C interface, with on-board Real-Time Clock, and user connections on 0.1” header
- SPI interface, with on-board Temperature measurement, and user connections on 0.1” header
- Large number of header and jumper connections for configuration of the board
- Push Button for *RESET*
- LED indicators for *POWER, ERRORN, WATCHDOG* and *PROM_BUSY*

1.2 References

RD-1 GR712-BOARD_schematic.pdf, Schematic

RD-2 GR712-BOARD_assy_drawing.pdf, Assembly Drawing

RD-3 GR712RC Dual Core Leon3FT SparcV8 Processor, Datasheet

RD-4 GR712RC Dual Core Leon3FT SparcV8 Processor, User Manual

RD-5 GR-MEZZ Technical Note, Technical Note about Mezzanine connectors

1.3 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

ATTENTION! To prevent damage to board, please ensure that the correct power supply and power supply polarity is used with the board.

1.4 Abbreviations

ASIC	Application Specific Integrated Circuit.
DIL	Dual In-Line
ESD	Electro-Static Discharge
FT	Fault-Tolerant
GEO	Geostationary Earth Orbit
GPIO	General Purpose Input / Output
I/O	Input/Output
IP	Intellectual Property
LEO	Low Earth Orbit
LVDS	Low Voltage Digital Signalling
MUX	Multiplexer
PCB	Printed Circuit Board
RMII	Reduced Media Independent Interface
RS	Reed Solomon
SMD	Surface Mount Device
SPW	Spacewire
TMTC	Telemetry/Telecommand

2 ELECTRICAL DESIGN

2.1 GR712RC ASIC

The GR712RC ASIC is an advanced system on a chip, with advanced interface protocols, dedicated for high reliability Rad-Hard space, aeronautics and military applications. The GR712RC incorporates a dual core LEON3-FT SPARC V8 processor architecture and its internal block diagram is represented in Figure 2-1.

In order to reduce the number of pins required on the device, an internal programmable switch matrix allows the same pin to be used for difference interface functions.

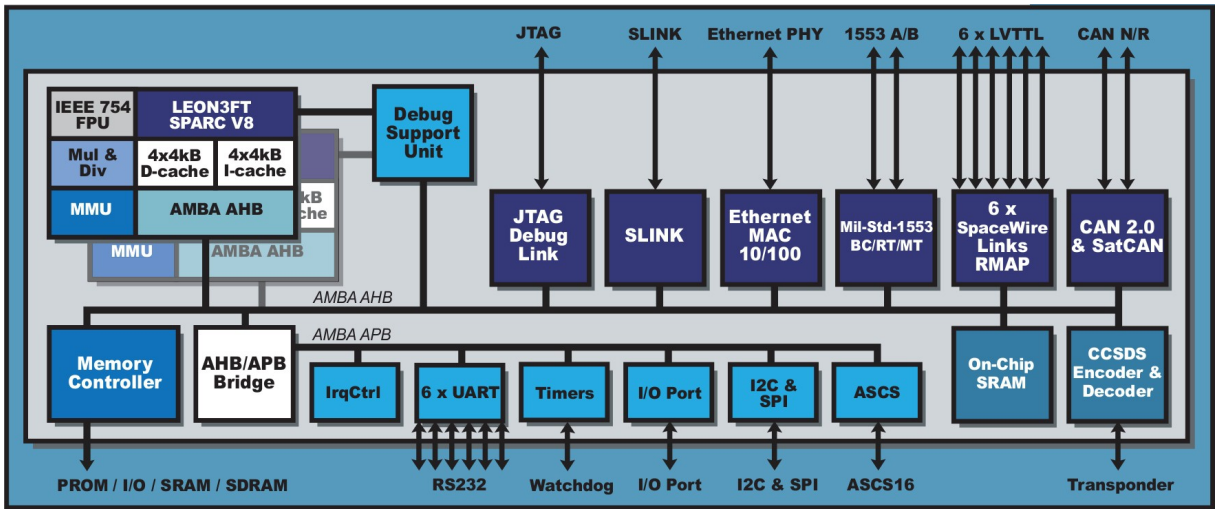

Figure 2-1: GR712RC ASIC Block Diagram

The GR712RC ASIC is packaged in a 240-pin, 0.5mm pitch Ceramic Quad Flatpack, and is soldered on to the PCB.

Details of the interfaces, operation and programming of the GR712RC ASIC is given in the *GR712 Datasheet,* RD-3, and *User Manual*, RD-4.

Figure 2-2: GR712RC ASIC

2.2 Block Diagram

The *GR712-BOARD* provides the electrical functions and interfaces as represented in the block diagram, Figure 2-3.

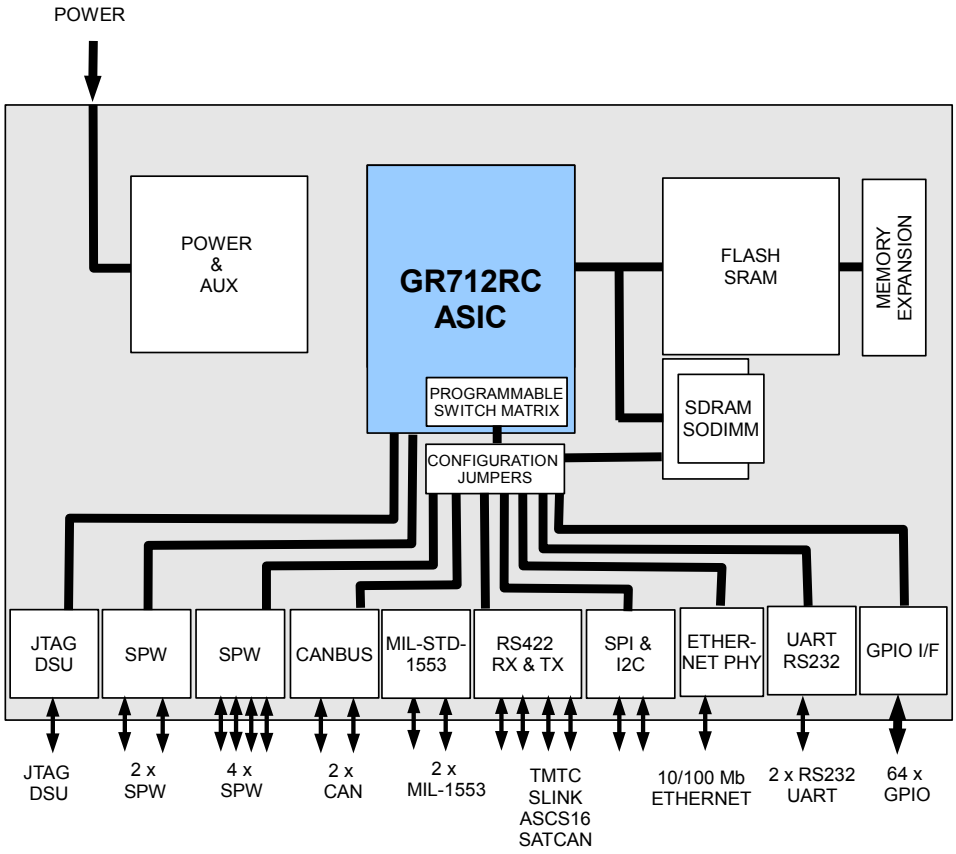

Figure 2-3: Block Diagram of GR712-BOARD

The Main PCB is of standard Double Eurocard format (233.35 x 160mm) and can be used 'stand-alone' on the bench-top simply using an external +5V power supply. The board is compatible with mounting in a 6U Compact PCI rack, if a suitable front panel is mounted.

2.3 Memory

The memory configuration installed on the board is shown in the figure below comprising of:

- 80Mbit of SRAM memory, organised as 1 bank x 2Mword x 40 bits wide

  (a second SRAM bank can be installed on the PCB, but is not fitted as standard)
- 64Mbit of Flash PROM, organised as 1 bank x 8 Mword x 8 bits wide)
- SODIMM socket to allow up to 64Mword x 48 bit SDRAM to be installed with 512Mbyte module

Additionally, in order to allow users to install alternative memory configurations or devices, all the signals of the memory interface are connected to memory expansion connectors. The expansion connectors allow mezzanine boards to be added similar to those developed for the existing *GR-CPCI* development boards.

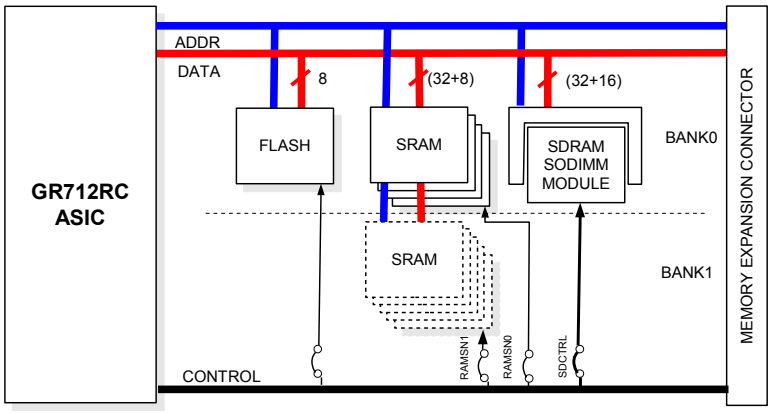

Figure 2-4: On-Board Memory Configuration

2.3.1 SRAM

The *GR712-BOARD* is laid out with two SRAM memory banks but only has one bank mounted as standard. Each bank is made up of five *CY7C1069AV33*. These devices are 16Mbit (2Mbyte x 8 bit) devices with 10 or 12 ns access times.

The five devices provide (32 + 8) bit wide SRAM memory paths allowing EDAC operation.

These memory banks are mapped as RAMBANK0 and RAMBANK1.

In case the user wishes to disable the on board memory, this can be done by removing the jumpers *JP76* on the PCB.

2.3.2 FLASH

The *GR712-BOARD* has mounted as standard one FLASH memory bank, made up of one Intel *JS28F640J3* FLASH device. This device is a 64Mbit (8Mbyte x 8 bit device), typically with 90ns access times. The data bus width to the Flash memory is 8 bits wide.

Note that, the PROM width and PROM EDAC conditions are set by the state of the GPIO[3] and GPIO[1] pins at power up of the Processor. These pins are provided with pull-down resistors to set the default mode to *8 bit* with *no EDAC*. If EDAC operation of the Flash Prom is desired, then jumper JP85 should be installed, to pull-up GPIO[1].

If measuring the state of the GPIO pins, please take into account the effect of these pull-down resistors. Conversely, if an external signal is connected to the GPIO[3] and GPIO[1] pins, this may override the expected state of the pin at power up.

For more information on the *PROM-width* and *PROM-EDAC* settings, refer to the Memory Configuration documentation in the GR712RC User Manual, RD-4.

2.3.3 SDRAM

Standard PC133 SDRAM can be installed by means of an 144 pin SO-DIMM socket on-board. The SO-DIMM provides 64 bit wide data paths. However, in the standard Leon model only 32 data bits of the SDRAM are used, plus 16 additional data bits for the RS/EDAC memory bits.

Therefore nominally only half the capacity of the SO-DIMM will be available.

Note: the SDRAM interface is limited to 80 MHz, and will not operate when the GR712RC is clocked at 96 MHz using the 2x48 MHz DLL mode. To operate the SDRAM, run the device at 48 MHz from X1, or at 80 MHz using the supplied 80 MHz oscillator in X2.

2.3.4 Expansion Connector

To make it feasible for users to define peripherals mapped in the processor I/O space and implement mezzanine boards which could be connected to this Development Board in a similar manner to the other GR Development Boards, the memory bus signals of the GR712 processor are connected to a 120 pin AMP connector (*AMP 5-177984-5), J9* and 60 pin connector (AMP 5-177984-2)*, J11*

Table 4-12 and Table 4-14 list the signals and their pin numbers for these connectors.

Figure 2-5 shows the pin numbering scheme as implemented on the expansion connector.

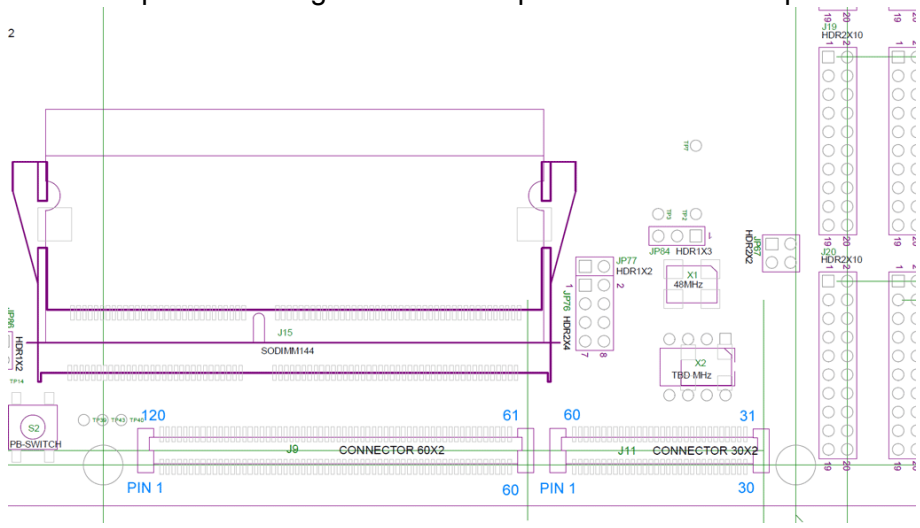

Figure 2-5: Mezzanine Connector Pin Number Ordering

Please note that this pin ordering does not match exactly the pin ordering which you will find on the Tyco part datasheets for the Mezzanine board mating connectors. The reason for this is explained in more detail in the Technical Note, RD-5.

Therefore please take care when designing your own mezzanine boards to take account of this pin ordering.

If there is any confusion, or you have any doubts, please do not hesitate to contact info@pender.ch. Additional dimensional data or Gerber layout information can be provided, if required to aid in the layout of the User's mezzanine board.

2.4 Switch Matrix for I/O

The programmable switch matrix inside the GR712RC device allows the same pin to be used for different interface functions. Figure 2-6 shows the multiple interface functions which are assigned to the Switch Matrix I/O pins on the GR712RC device. Different interface types are grouped and highlighted by colour.

For the definition and explanation of the pin names, please refer to the Data Sheet for the GR712RC Device, RD-3.

JUMPER POS.:	'A' = 1-2	'B' = 3-4	'C' = 5-6	'D' = 7-8	'E' = 9-10	'F' = 11-12		
	GPIO	CF0 GEO CPU	CF1 TM/TC	CF2 LEO CPU	CF3 INSTR CTL A	CF4 INSTR CTL B	U1B	
		UART_TX0	UART_TX0	UART_TX0	UART_TX0	UART_TX0	SWMX_00	4
		UART_RX0	UART_RX0	UART_RX0	UART_RX0	UART_RX0	SWMX_01	3
		UART_TX1	UART_TX1	UART_TX1	UART_TX1	UART_TX1	SWMX_02	2
	GPIO_0	UART_RX1	UART_RX1	UART_RX1	UART_RX1	UART_RX1	SWMX_03	1
	GPIO_1	UART_TX2	UART_TX2	UART_TX2	UART_TX2	UART_TX2	SWMX_04	240
	GPIO_2	UART_RX2	UART_RX2	UART_RX2	UART_RX2	UART_RX2	SWMX_05	239
	GPIO_3	UART_TX3	UART_TX3	UART_TX3	UART_TX3	UART_TX3	SWMX_06	238
	GPIO_4	UART_RX3	UART_RX3	UART_RX3	UART_RX3	UART_RX3	SWMX_07	233
	GPIO_5	UART_TX4	TMDO	UART_TX4	UART_TX4	UART_TX4	SWMX_08	232
	GPIO_6	UART_RX4	TMCLKI	UART_RX4	UART_RX4	UART_RX4	SWMX_09	231
	GPIO_7	UART_TX5	TMCLKO	UART_TX5	UART_TX5	UART_TX5	SWMX_10	230
	GPIO_8	UART_RX5	TCACT0	UART_RX5	UART_RX5	UART_RX5	SWMX_11	229
	GPIO_9	SPWTXS_4	SDCSN[0]	SDCSN[0]	SDCSN[0]	SDCSN[0]	SWMX_12	228
	GPIO_10	SPWTXD_4	SDCSN[1]	SDCSN[1]	SDCSN[1]	SDCSN[1]	SWMX_13	227
	GPIO_11	SPWRXS_4	TCCLK0	A16DASA			SWMX_14	226
	GPIO_12	SPWRXD_4	TCD0	A16DASB			SWMX_15	225
	GPIO_13	SPWTXS_2	SPWTXS_2	CANTXA	CANTXA	SPWTXS_2	SWMX_16	220
	GPIO_14	SPWTXD_2	SPWTXD_2	CANTXB	CANTXB	SPWTXD_2	SWMX_17	219
	GPIO_15	SPWRXS_2	SPWRXS_2	CANRXA	CANRXA	SPWRXS_2	SWMX_18	218
	GPIO_16	SPWRXD_2	SPWRXD_2	CANRXB	CANRXB	SPWRXD_2	SWMX_19	217
	GPIO_17	SPWTXS_3	SPWTXS_3	SLSYNC	SLSYNC	SPWTXS_3	SWMX_20	203
	GPIO_18	SPWTXD_3	SPWTXD_3	A16ETR		SPWTXD_3	SWMX_21	202
	GPIO_19	SPWRXS_3	SPWRXS_3			SPWRXS_3	SWMX_22	201
	GPIO_20	SPWRXD_3	SPWRXD_3			SPWRXD_3	SWMX_23	200
	GPIO_21	SPWTXD_5	SDDQM[0]	SDDQM[0]	SDDQM[0]	SDDQM[0]	SWMX_24	197
	GPIO_22	SPWTXS_5	SDDQM[1]	SDDQM[1]	SDDQM[1]	SDDQM[1]	SWMX_25	196
	GPIO_23	SPWRXS_5	TCRFAVL0	STCNEX0	STCNEX0		SWMX_26	193
	GPIO_24	SPWRXD_5	TCCLK1	STCNEX1	STCNEX1		SWMX_27	192
	GPIO_25	1553RXENA		STCNCLK1M	STCNCLK1M	RMTXD0	SWMX_28	191
	GPIO_26	1553TXA		STCNMRK1	STCNMRK1	RMTXD1	SWMX_29	190
	GPIO_27	1553RXA	TCD1	STCNEX2	STCNEX2	RMRXD0	SWMX_30	189
	GPIO_28	1553RXNA	TCACT1	STCNCLS1M	STCNCLS1M	RMRXD1	SWMX_31	188
	GPIO_29	1553TXNA		STCNMRK2	STCNMRK2	RMTXEN	SWMX_32	185
	GPIO_30	1553TXINHA		STCNMRK3	STCNMRK3		SWMX_33	184
	GPIO_31	1553RXB	TCRFAVL1	STCNTOD1N	STCNTOD1N	RMCRSDV	SWMX_34	183
	GPIO_32	1553RXNB	TCCLK2	STCNTOD2N	STCNTOD2N	RMINTN	SWMX_35	182
	GPIO_33	1553RXENB		A16MCS		RMMDIO	SWMX_36	179
	GPIO_34	1553TXB		A16HS		RMMDC	SWMX_37	178
	GPIO_35	1553CLK	TCD2			RMRFCLK	SWMX_38	177
	GPIO_36		TCACT2	STCNPPS1N	STCNPPS1N		SWMX_39	176
	GPIO_37	1553TXNB		A16DCS			SWMX_40	175
	GPIO_38	1553TXINHB		A16MAS			SWMX_41	174
	GPIO_39		TCRFAVL2	STCNPPS2N	STCNPPS2N		SWMX_42	173
	GPIO_40			STCNSYNC	STCNSYNC		SWMX_43	172
	GPIO_41	SPICLK		SLO	SLO	SPICLK	SWMX_44	169
	GPIO_42	SPIMOSI		SLCLK	SLCLK	SPIMOSI	SWMX_45	166
	GPIO_43		TCCLK3				SWMX_46	165
	GPIO_44		TCD3				SWMX_47	164
	GPIO_45		SDCAS	SDCASN	SDCASN	SDCASN	SWMX_48	163
	GPIO_46		SDRAS	SDRASN	SDRASN	SDRASN	SWMX_49	162
	GPIO_47		TCACT3				SWMX_50	161
	GPIO_48	SPIMISO	TCRFAVL3	SLI	SLI	SPIMISO	SWMX_51	160
	GPIO_49		SDWEN	SDWEN	SDWEN	SDWEN	SWMX_52	157
	GPIO_50		SDDQM[2]	SDDQM[2]	SDDQM[2]	SDDQM[2]	SWMX_53	155
	GPIO_51		SDDQM[3]	SDDQM[3]	SDDQM[3]	SDDQM[3]	SWMX_54	154
	GPIO_52		TCACT4				SWMX_55	153
	GPIO_53		TCRFAVL4				SWMX_56	144
	GPIO_54	I2CSDA	TCCLK4	I2CSDA	I2CSDA	I2CSDA	SWMX_57	143
	GPIO_55	I2CSCL	TCD4	I2CSCL	I2CSCL	I2CSCL	SWMX_58	142
	GPIO_56		CB[8]	CB[8]	CB[8]	CB[8]	SWMX_59	140
	GPIO_57		CB[9]	CB[9]	CB[9]	CB[9]	SWMX_60	137
	GPIO_58		CB[10]	CB[10]	CB[10]	CB[10]	SWMX_61	136
	GPIO_59		CB[11]	CB[11]	CB[11]	CB[11]	SWMX_62	135
	GPIO_60		CB[12]	CB[12]	CB[12]	CB[12]	SWMX_63	132
	GPIO_61		CB[13]	CB[13]	CB[13]	CB[13]	SWMX_64	129
	GPIO_62		CB[14]	CB[14]	CB[14]	CB[14]	SWMX_65	128
	GPIO_63		CB[15]	CB[15]	CB[15]	CB[15]	SWMX_66	127

Figure 2-6: Switch Matrix and Interface Functions

As can be seen from Figure 2-6, five basic interface configurations are defined for the GR712RC device:

CF0	GEOCPU	Processor for GEO applications
CF1	TMTC	Processor for TMTC applications
CF2	LEOCPU	Processor for LEO applications
CF3	INSTR CTRL A	Instrument Controller, type A
CF4	INSTR CTRL B	Instrument Controller, type B

If not otherwise used, a pin can be defined as a standard general purpose I/O for user-defined use.

In order to be able to configure the *GR712-BOARD* to operate in all these configurations, each Switch Matrix pin on the GR712RC ASIC is connected to a 12 pin, 2mm pitch header as represented in Figure 2-7.

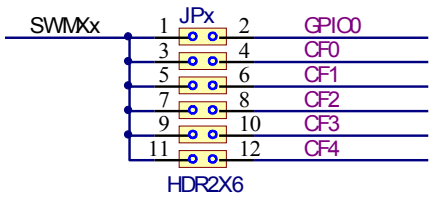

Figure 2-7: Configuration Jumpers

If the pin is to be used as a General Purpose I/O pin, the jumper would be inserted in the position 1-2. If the pin is to be used for configuration type CF0, the jumper would be inserted in the position 3-4, and so on.

Please note that on the silkscreen printing on the actual PCB, the jumper positions are marked with the letters 'A' to 'F' which correspond as follows:

'A' = 1-2

'B' = 3-4

'C' = 5-6

'D' = 7-8

'E' = 9-10

'F' = 11-12

In this simple manner the interface can be freely and flexibly configured, but the User must take care to ensure that the jumpers are set in the correct position to suit the interface functions they require.

2.5 CAN Interface

The board provides the electrical interfaces for two CAN bus interfaces, as represented in the block diagram, Figure 2-8.

The CAN bus transceiver IC's on this board are *SN65HVD230* devices from Texas Instruments which operate from a single +3.3V power supply.

The connector interfaces are male DSUB-9 connectors adhering to the standard pin-out for this type of interface (ref. Table 4-5 And Table 4-4).

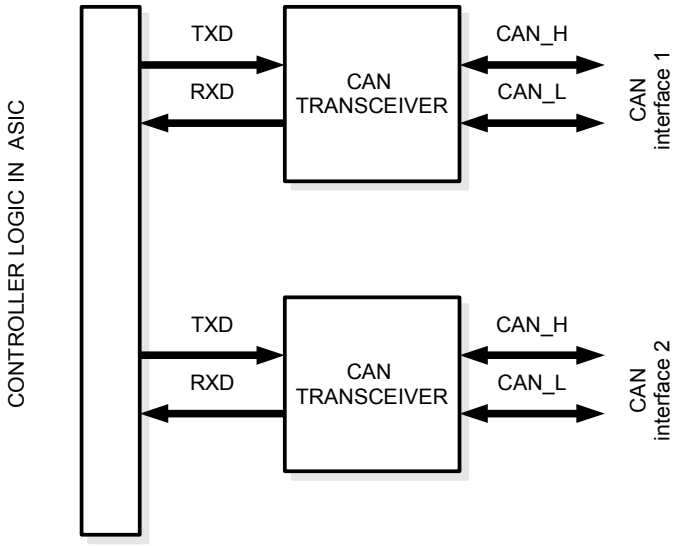

Figure 2-8: Block Diagram of the CAN interface

2.5.1 Configuration of Bus Termination

The CAN interfaces on the board can be configured for either end node or stub-node operation by means of the jumpers JP78 and JP79 for interface 1 and 2 respectively, as shown in Figure 2-9.

For normal end-node termination with a nominal 120 Ohm insert jumpers in position 1-3.

However, if a split termination is desired (if required for improved EMC performance), insert the jumpers in positions 1-2 and 3-4.

For stub nodes, if termination is not required, do not install any jumpers.

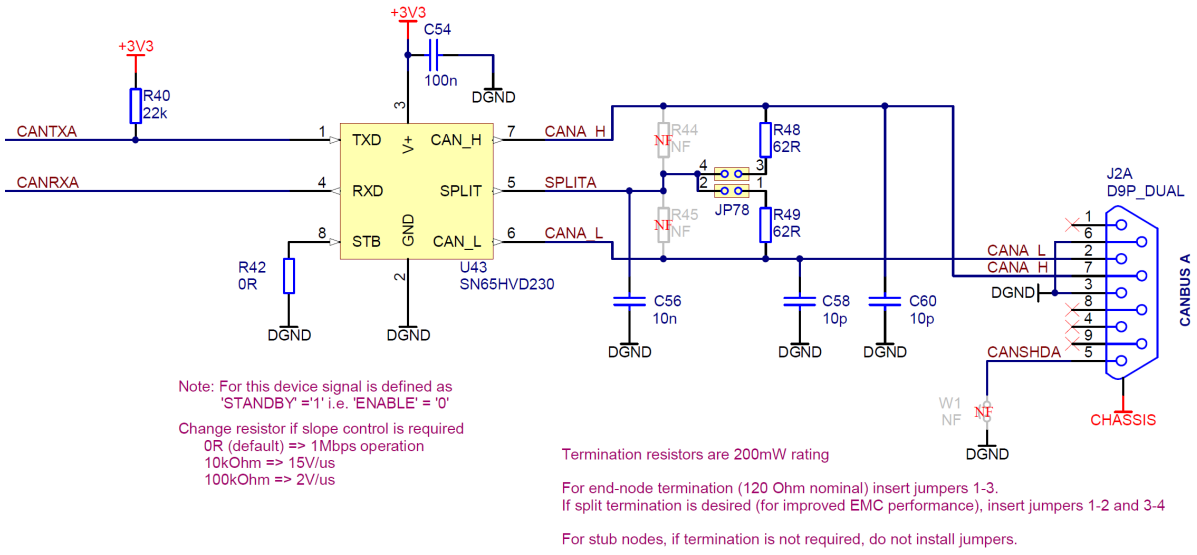

Figure 2-9: Transceiver and Termination Configuration (one of 2 interfaces shown)

2.5.2 Configuration of Slew Rate

The SN65HVD230 transceiver device used on the board has the facility to set the device into *STANDBY* mode, by connecting an active high external signal to pin 8 of the device. However, on this board this is tied to permanently *'low'* to enable the CAN bus Transceivers.

A further feature provided by the SN65HVD230 device is the capability to adjust the transceiver slew rate. This can be done by modifying the values of resistors connected to pin 8 of the transceivers.

The default value of 0 ohms is compatible with 1Mbps operation.

From the data sheet the following resistor values give the following slew rates:

10kOhm => 15V/us

100kOhm => 2V/us

2.6 Spacewire (LVDS) Interfaces

The *GR712RC ASIC* provides six Spacewire interfaces which are routed to connectors of the the board. Two interfaces *SPW-0* and *SPW-1* are dedicated Spacewire interfaces. The four remaining interfaces *SPW-2 – SPW5* are available if the Switch matrix is suitably configured.

2.6.1 SPW interface circuit

Each Spacewire interface consists of 4 LVDS differential pairs (2 input pairs and 2 output pairs), as shown in the figure below. As the Spacewire interface to the *GR712RC ASIC* is LVTTL (3.3V logic), LVDS driver and receiver circuits are required on the PCB to interface between the ASIC and the external interface.

The PCB traces for the LVDS signals on the *GR712-BOARD* are laid out with 100-Ohm differential impedance design rules and matched trace lengths.

100 Ohm Termination resistors for the LVDS receiver signals are mounted on the board close to the receiver.

The pin out and connector types for these Spacewire interfaces conform to the Spacewire standard, as shown in Figure 2-10.

The inner shield pin (pin3 of the connector) is connected to DGND via a 10kohm resistor.

2.6.2 SPWCLK

Configuration options on the board (jumpers, crystal socket and SMA coaxial connector) allow this Spacewire clock to be provided from the following sources:

- Dedicated *SPWCLK* oscillator (if appropriate Oscillator X5 is mounted in socket and jumper JP88 is not installed)
- Main processor oscillator X1(if jumper JP88 is installed)
- External clock input via SMA connector J31. (X5 and JP88 not installed)

The default configuration is that the clock is supplied by the Main processor oscillator X1, and jumper JP88 is installed. Do not install jumper JP88 if an oscillator is installed in X5 socket as this will unintentionally connect the outputs of oscillator X1 and Oscillator X5 together.

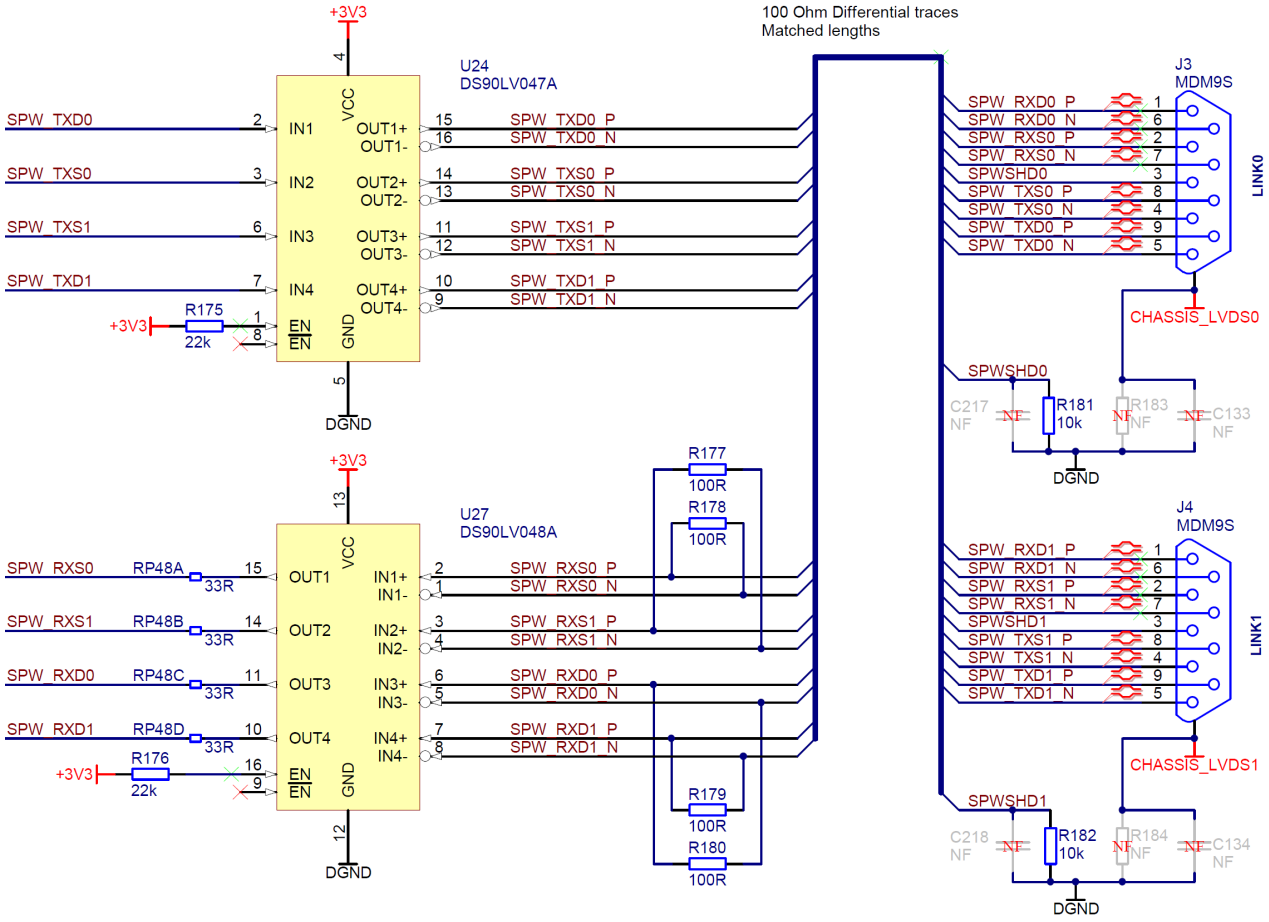

Figure 2-10: Transceiver and Termination of the SPW interfaces (2 of 6 interfaces shown)

At power-up or reset of the board, the SpaceWire Clock Divisor Registers values are cleared to zero, except the following bits which are taken from the GPIO inputs:

- bits 8 & 0 are set by the state of GPIO[34]
- bits 9 & 1 are set by the state of GPIO[37]
- bits 10 & 2 are set by the state of GPIO[40]
- bits 11 & 3 are set by the state of GPIO[42]

On the *GR712-BOARD* resistors can be installed in order to set these pins by means of either a pull-up (logic '1') or a pull-down (logic '0') resistor, as shown in the figure below.

The Pads for the Pull-down resistors are on the top side of the PCB, and the pads for the Pull-up resistors are on the bottom side of the PCB.

The default when delivered is that the pull-down resistors are mounted.

Note that, elsewhere on the board, each GPIO already has a weak pull-up (47kOhm) resistor, to ensure that the pins are not unintentionally left floating. The value of the pull-down resistor must be selected to be sufficiently strong to override the effect of this pull-up.

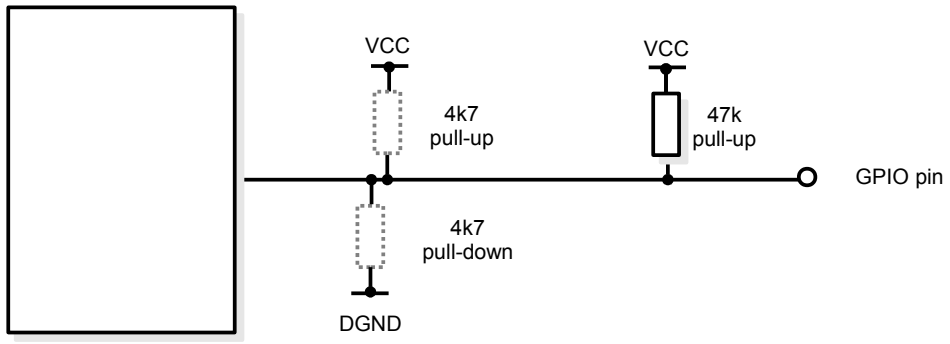

Figure 2-11: SPW Clock Divisor Configuration Resistors

GPIO Pin	ASIC pin name	Pull-down Resistor	Pull-up Resistor	Comment
GPIO[34]	SWMX37	R212	R221	R212 (4k7) is fitted as default
GPIO[37]	SWMX40	R211	R220	R211 (4k7) is fitted as default
GPIO[40]	SWMX43	R210	R219	R210 (4k7) is fitted as default
GPIO[42]	SWMX45	R209	R218	R209 (4k7) is fitted as default

Table 2-1: SpaceWire Clock Divisor Resistors

2.7 RS422 Interfaces for UART and TMTC functions

The GR712RC ASIC provides up to six UART interfaces, each with RXD/TXD pin pairs (3.3V TTL levels). For these interfaces RS422 transmitter/receiver have been defined.

Additionally, when defined for TMTC, ASCS16, SLNK and SATCAN functionality, RS422 signal levels are also required on a number of interfaces. The board therefore provides transmitter and receiver circuits for:

20 RS422 Transmitter Pairs

28 RS422 Receiver pairs

Since defining individual connector types for each combination of interfaces, while maintaining flexibility would lead to unmanageable complexity on the board, the RS422 signals are instead simply routed to a set of standard 0.1” pin headers.

If the connector type and pin-out interfaces is known, an appropriate wire harness can be easily defined to accommodate the desired connector types.

2.7.1 RS422 Transmitter Circuits

Each transmitter pair is connected to an 3.3V RS422 Transmitter circuit as shown in Figure 2-12

Some of the TMTC interface types require series 100 Ohm resistors for source-series termination of the interface. This can be provided on an individual basis for the transmitter pairs by means of series resistors installed on the board close to the transmitter circuits. If source-series termination is not required then zero-ohm resistors should be installed for the RS422 transmitter interfaces.

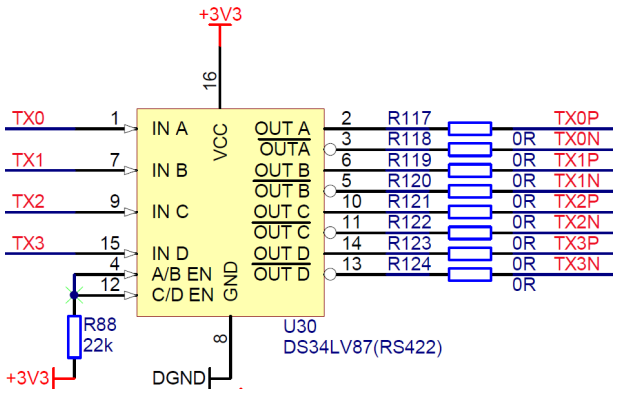

Figure 2-12: RS422 TX configuration

2.7.2 RS422 Receiver Circuits

Each receiver pair is connected to an 3.3V RS422 Receiver circuit as shown in Figure 2-13.

In the default configuration, none of the receiver pairs are provided with any form of termination. However, this can be added on an individual basis. Either an AC or simple resistive termination can be installed.

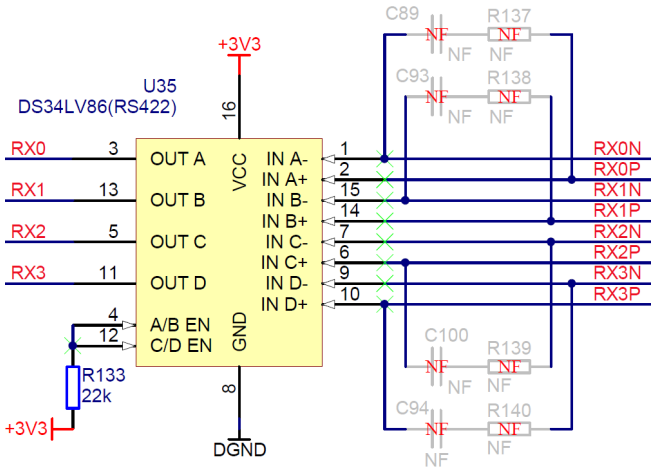

Figure 2-13: RS422 Receiver Configuration

2.8 UART's

The *GR712RC ASIC* incorporates a IP core which implement standard serial UART functionality. The interface to this core consists of the following as listed in Table 2-2.

These signals are defined to have RS422 voltage levels and 'share' connector pin as shown in the last column of the table

Name	Pin	Direction	Function	'Shares'
UARTTX0	4 / SWMX0	Out	Transmit 0	RS422_TX_0
UARTTX1	3 / SWMX2	Out	Transmit 1	RS422_TX_1
UARTTX2	2 / SWMX4	Out	Transmit 2	RS422_TX_2
UARTTX3	1 / SWMX6	Out	Transmit 3	RS422_TX_3
UARTTX4	240 / SWMX8	Out	Transmit 4	RS422_TX_4
UARTTX5	239 / SWMX10	Out	Transmit 5	RS422_TX_5
UARTRX0	238 / SWMX1	In	Receive 0	RS422_RX_0
UARTRX1	233 / SWMX3	In	Receive 1	RS422_RX_1
UARTRX2	232 / SWMX5	In	Receive 2	RS422_RX_2
UARTRX3	231 / SWMX7	In	Receive 3	RS422_RX_3
UARTRX4	230 / SWMX9	In	Receive 4	RS422_RX_4
UARTRX5	229 / SWMX11	In	Receive 5	RS422_RX_5

Table 2-2: List of UART Signals

2.9 ASCS16

The *GR712RC ASIC* incorporates a IP core which implements ASCS16 (STR) functionality. The interface to this core consists of the following as listed in Table 2-3.

These signals are defined to have RS422 voltage levels and 'share' connector pin as shown in the last column of the table

Name	Pin	Direction	Function	'Shares'
A16DASA	226 / SWMX14	In		RS422_RX_6
A16DASB	225 / SWMX15	In		RS422_RX_7
A16MCS	179 / SWMX36	Out		RS422_TX_8
A16HS	178 / SWMX37	Out		RS422_TX_9
A16DCS	175 / SWMX40	Out		RS422_TX_10
A16MAS	174 / SWMX41	Out		RS422_TX_11
A16ETR	202 / SWMX21	Out		RS422_TX_7

Table 2-3: List of ASCS16 Signals

2.10 SLINK

The *GR712RC ASIC* incorporates a IP core which implements SLINK (6MHz serial port) functionality. The interface to this core consists of the following as listed in Table 2-4.

These signals are defined to have RS422 voltage levels and 'share' connector pin as shown in the last column of the table

Name	Pin	Direction	Function	'Shares'
SLI	160 / SWMX51	In		RS422_RX_20
SLO	169 / SWMX44	Out		RS422_TX_12
SLSYNC	203 / SWMX20	Out		RS422_TX_6
SLCLK	166 / SWMX45	Out		RS422_TX_13

Table 2-4: List of SLINK Signals

2.11 TMTC

The *GR712RC* ASIC incorporates a IP core which implements TMTC functionality. The interface to this core consists of the following as listed in Table 2-5. These signals are defined to have RS422 voltage levels and 'share' connector pin as shown in the last column of the table.

Name	Pin	Direction	Function	'Shares'
TMDO	232 / SWMX8	Out		RS422_TX_4
TMCLKO	230 / SWMX10	Out		RS422_TX_5
TMCLKI	231 / SWMX9	In		RS422_RX_4

Name	Pin	Direction	Function	'Shares'
TCD0	225 / SWMX15	In		RS422_RX_7
TCD1	189 / SWMX30	In		RS422_RX_10
TCD2	177 / SWMX38	In		RS422_RX_14
TCD3	164 / SWMX47	In		RS422_RX_18
TCD4	142 / SWMX58	In		RS422_RX_24
TCCLK0	226 / SWMX14	In		RS422_RX_6
TCCLK1	192 / SWMX27	In		RS422_RX_9
TCCLK2	182 / SWMX35	In		RS422_RX_13

Name	Pin	Direction	Function	'Shares'
TCCLK3	165 / SWMX46	In		RS422_RX_17
TCCLK4	143 / SWMX57	In		RS422_RX_23
TCACT0	229 / SWMX11	In		RS422_RX_5
TCACT1	188 / SWMX31	In		RS422_RX_11
TCACT2	176 / SWMX39	In		RS422_RX_15
TCACT3	165 / SWMX46	In		RS422_RX_19
TCACT4	143 / SWMX57	In		RS422_RX_21
TCRFAVL0	193 / SWMX26	In		RS422_RX_8
TCRFAVL1	183 / SWMX34	In		RS422_RX_12
TCRFAVL2	173 / SWMX42	In		RS422_RX_16
TCRFAVL3	160 / SWMX51	In		RS422_RX_20
TCRFAVL4	144 / SWMX56	In		RS422_RX_22

Table 2-5: List of TMTC Signals

2.12 Serial Interface (RS232)

The *GR712-BOARD*, provides RS232 interface circuits and connectors for two Serial interfaces with TXD/RXD pins. This interface shares the TX0/RX0 and TX1/RX1 pin pairs with the RS422 interface, and therefore it is necessary to set jumpers JP1 and JP2 to select either RS422 (Install jumpers 1-3 and 2-4) or RS232 (jumpers 3-5 and 4-6) – Refer to Schematic, RD-1.

The front panel connector type for the UART interfaces is a Female D-Sub 9 pin type with a standard pin-out for serial links.

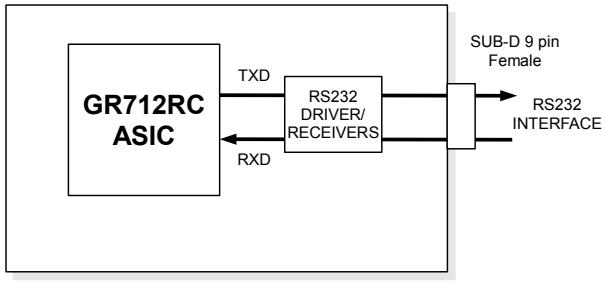

Figure 2-14: Serial interface

2.13 Debug Support Unit (DSU) Serial Interface

The *GR712-BOARD* provides a interface for Debug and control of the processor by means of a host terminal via the DSU JTAG link to the *GR712RC ASIC*, as represented in Figure 2-15. The connection to the board is via the Mini-USB connector J12, and the translation between USB and JTAG signals of the ASIC is performed via a FT2232H, Hi-Speed Dual USB UART/FIFO IC.

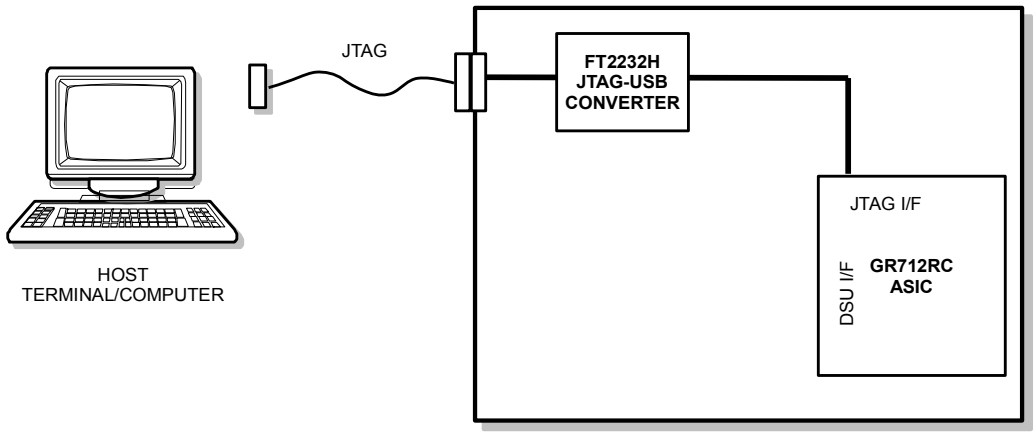

Figure 2-15: Debug Support Unit connections

On this chip there is no *DSUEN* signal so the DSU is always enabled to allow processor control and program debugging via the DSU link.

On this chip there is no *DSUACT* signal to indicate the DSU operation state.

On this chip there is no *DSUBREAK* signal.

2.14 Oscillators and Clock Inputs

The oscillator and clock scheme for the *GR712-BOARD* is shown in Figure 2-16.

2.14.1 Main Clock

The main oscillator for the *GR712RC ASIC* is a 48 MHz Crystal oscillator. This oscillator is an SMD oscillator soldered on to the board.

If a different user defined main operating frequency is required, this can be achieved by installing a 4 pin 3.3V/DIL8 style oscillator, in socket X2 on the board and moving jumper JP84.

A zero-delay buffer circuit (CY2305) is used to distribute the MAINCLK.

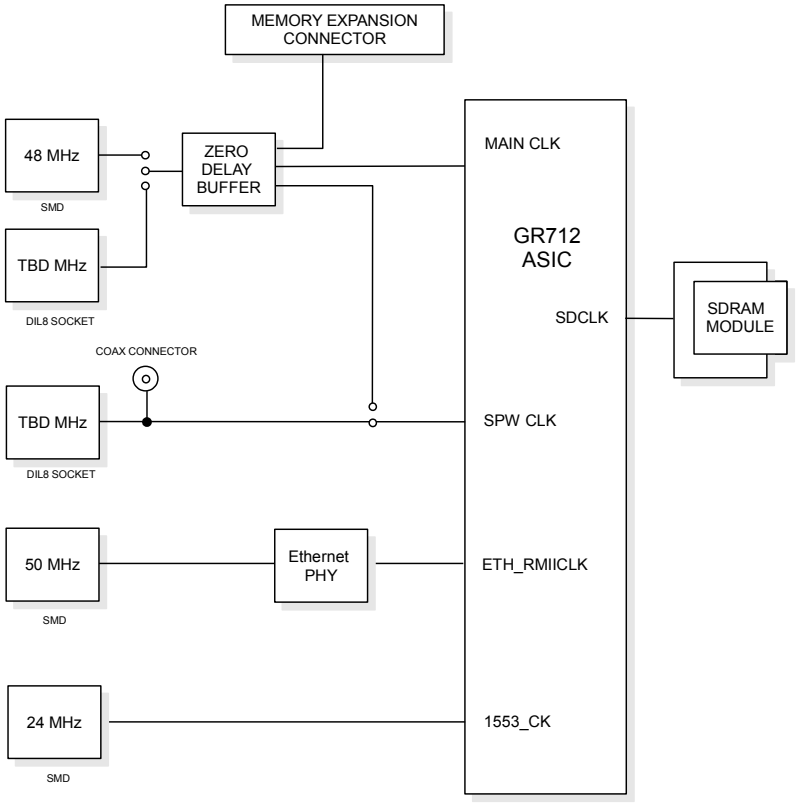

Figure 2-16: Clock Distribution Scheme

2.14.2 SPW_CLK

The *SPWCLK* can be derived from either the MAIN CLK, a separate socketed on-board crystal oscillator, or can be injected on a SMA coaxial connector on the board.

2.14.3 Ethernet Clock

A dedicated 50MHz SMD oscillator is provided for the Ethernet Controller and PHY circuit (see section 2.16).

2.14.4 MIL-STD-1553 Interface Clock

A dedicated 24.0MHz SMD oscillator is provided for the MIL-STD-1553 interface logic in the ASIC.

2.15 Power Supply and Voltage Regulation

The board operates from a single +5V DC power supply input. On board regulators generate the following voltages:

- +3.3V for the GR712RC I/O voltage, memory chip and other peripherals
- +1.8V for GR712RC Vcore voltage

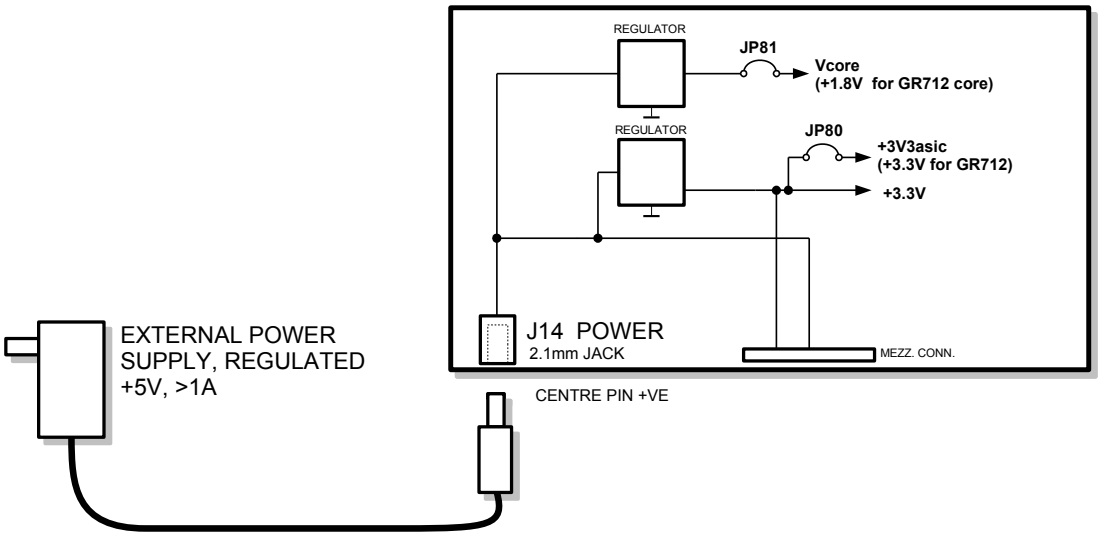

Figure 2-17: Power Regulation Configuration

Both the voltages +5V and +3.3V are provided to the memory expansion interface making feasible that user defined mezzanine boards can use these voltages.

The Jumpers JP80 and JP81 provide Current measurement points for monitoring and measurement of the current consumption of the GR712RC ASIC.

2.16 Ethernet Interface

The *GR712RC* ASIC device incorporates a Ethernet controller with support for RMII interface, and the *GR712* Development Board has a National Semiconductor DP83848 10/100Mbit/s Ethernet PHY transceiver and RJ45 connector are on board.

For more information on the registers and functionality of the Ethernet MAC+PHY device please refer to the data sheet for the *DP83848* device.

A 50 MHz oscillator dedicated for this device is provided on the board.

The interrupt output of the Ethernet MDIO interface is connected to the SWMX35 input to the *GR712RC ASIC*. This can be disabled by removing jumper *JP35-e* if necessary.

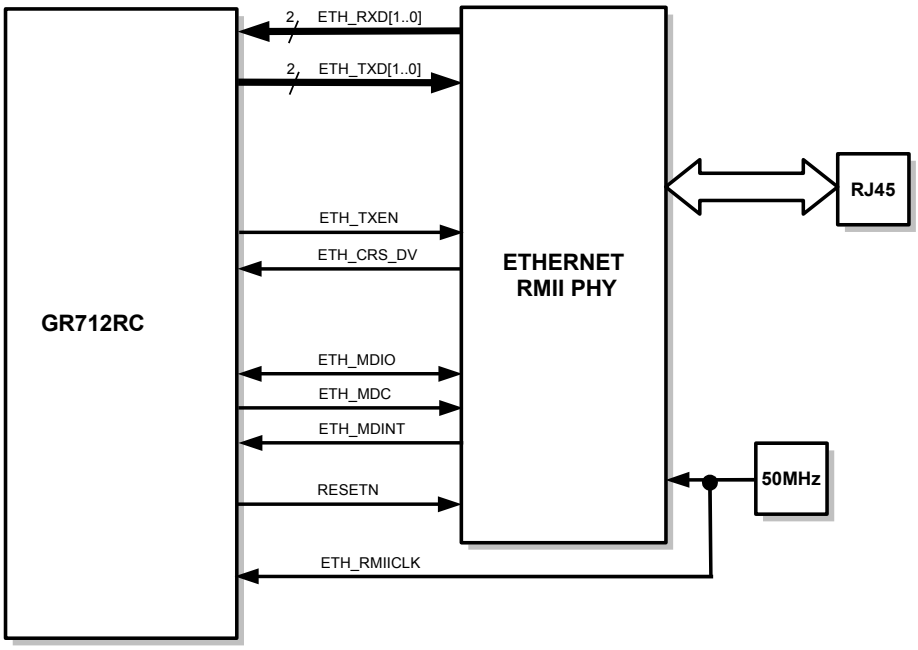

Figure 2-18: Block diagram of Ethernet RMII Interface

2.17 MIL-STD-1553 Interface

The board implements a Dual MIL-STD-1553 interface with a 3.3V Transceiver and Transformer circuits as shown in Figure 2-20.

Since there are various 'standard' connectors defined for the connection to MIL-STD-1553 bus, and because of limited PCB area it has instead been decided to implement a D9-Female connected for the connector on the board as this can be most easily adapted to suit the user's desired connector configuration.

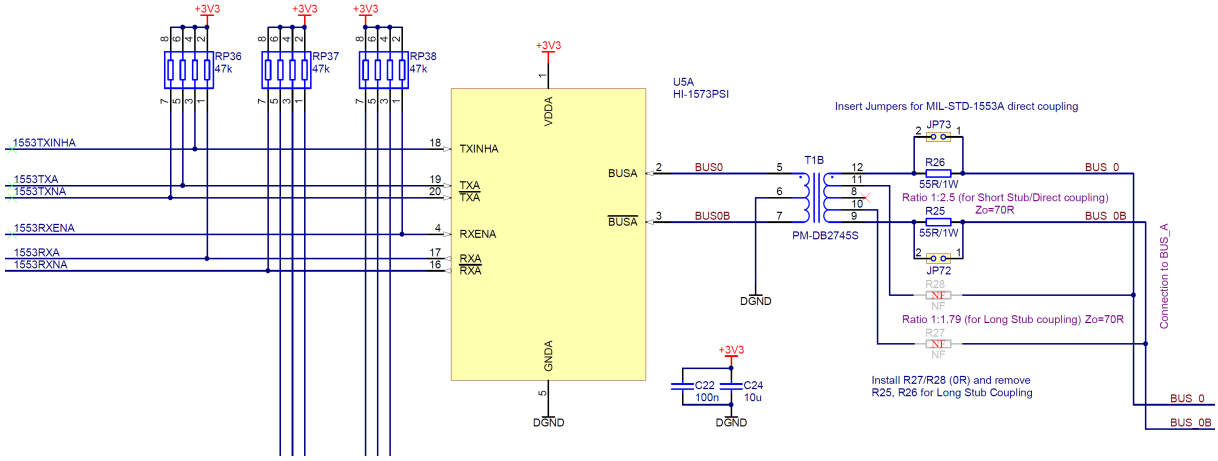

Figure 2-19: MIL-STD-1553 Transceiver and Transformer circuit
(one of two interfaces shown)

2.18 Other Interfaces and Circuits

2.18.1 GPIO

The 64 general Purpose Input Output signals of the ASIC (3.3V LVTTL voltage levels) are connected to a set of 0.1” pitch pin headers on the board, thus allowing easy access to these signals. A series protection resistor of 470 Ohm is included on each signal, and weak pull ups (47k) are provided on each of the signals lines on the PCB.

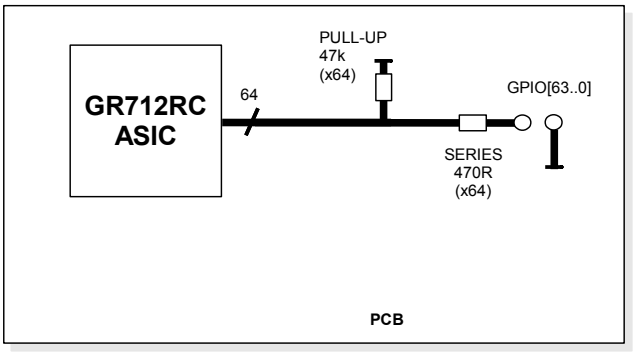

Figure 2-20: PIO interface configuration

Each GPIO signal has a corresponding ground pin on the pin header, thus allowing easy connection to ribbon cable or other external interfaces. If defined as inputs, the GPIO will have a default value of '1' (high) due to the Pull-up resistor, but can be set to '0' (low) by inserting a jumper over the corresponding Header pins.

Note that GPIO[31..0] correspond to the GR712RC pin function GPIO1[31..0], and GPIO[63..32] correspond to the GR712RC pin function GPIO2[31..0].

2.18.2 Reset Circuit and Button

A standard Processor Power Supervisory circuit (TPS3705 or equivalent) is provided on the Board to provide monitoring of the 3.3V power supply rail and to generate a clean reset signal at power up of the Unit.

To provide a manual reset of the board, a miniature push button switch is provided on the Main PCB for the control. Additionally connections are provided to an additional off-board push-button *RESET* switch if this is required.

2.18.3 Watchdog

The *GR712RC ASIC* includes a Watchdog timer function which can be used for the purpose of generating a system reset in the event of a software malfunction or crash.

On this development board the *WDOGN* signal is connected as shown in the Figure 2-21 to the Processor Supervisory circuit.

To utilise the Watchdog feature, it is necessary to appropriately set-up and enable the Watchdog timer. Please consult the *GR712RC User Manual* (RD-4) for the correct register locations and details.

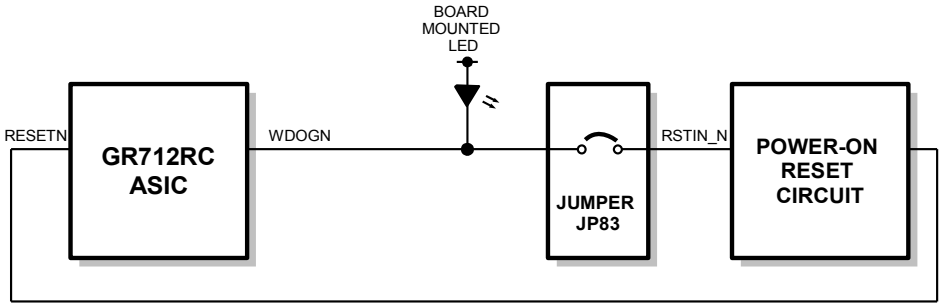

Figure 2-21: Watchdog configuration

Also, to allow the *WDOGN* signal to generate a system reset it is necessary to install the Jumper JP83 (see Figure 2-21).

For software development it is often convenient or necessary to disable the Watchdog triggering in order to be able to easily debug without interference from the Watchdog operation. In this case, the Jumper JP83 should be in the *removed*. When the watchdog triggers, the Watchdog LED will illuminate, but a system reset will not occur.

2.18.4 JTAG interface

The JTAG signals form the ASIC are connected to an FT2232HL interface chip. This chip provides a conversion to a standard USB interface on the front edge of the board (J12).

Special drivers in the GRMON debug software are able to communicate with this chip in order to enable a standard USB connection on a host computer to be used to perform the DSU Debug over the JTAG link of the ASIC.

2.18.5 I2C interface

As shown in Figure 2-22, the I2C interface pins of the GR712RC ASIC are connected to an 4 pin 0.1” header on the board, and Jumper JP70 allows pull-up resistors to be installed if the interface configuration requires them.

The GR712-BOARD provides an on-board DS1672 Real-Time Clock circuit, as an example I2C circuit.

2.18.6 SPI interface

As shown in Figure 2-23, the SPI interface pins of the GR712RC ASIC are connected to an 12 pin 0.1” header on the board. The SPI Chip Select pin is provided by an otherwise unused GPIO pin. Since the same pin is not available in all configurations, multiple GPIO pins are provided on the 12 pin header, and the User should choose an appropriate pin.

The GR712-BOARD provides an on-board AD7841, Temperature monitor circuit, as an example SPI circuit. The Chip Select for this device is provided by GPIO54.

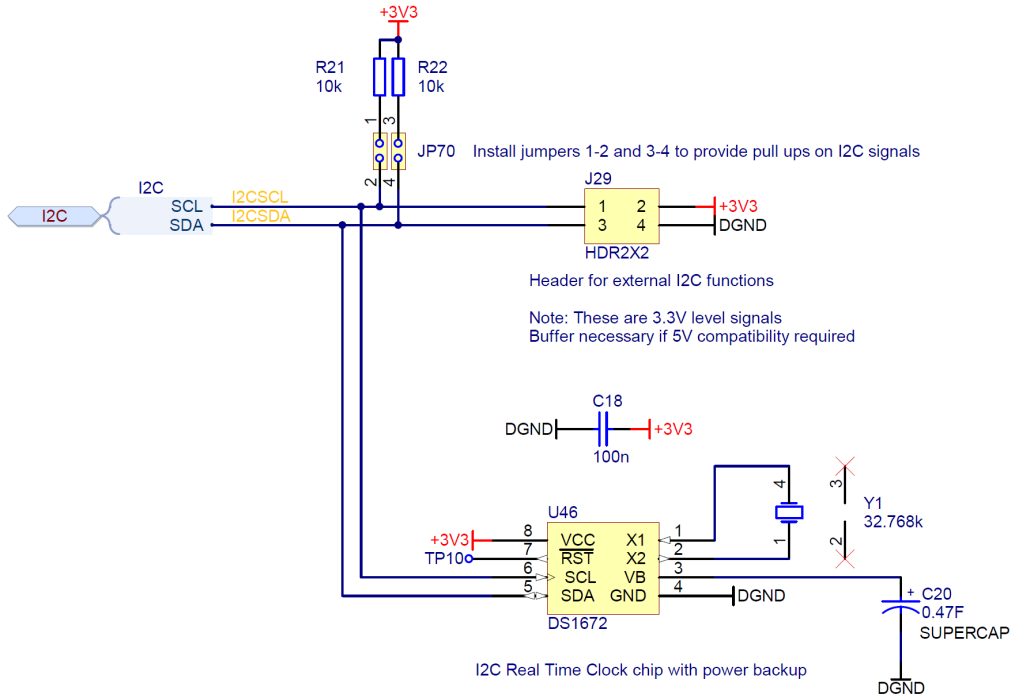

Figure 2-22: I2C Interface Configuration

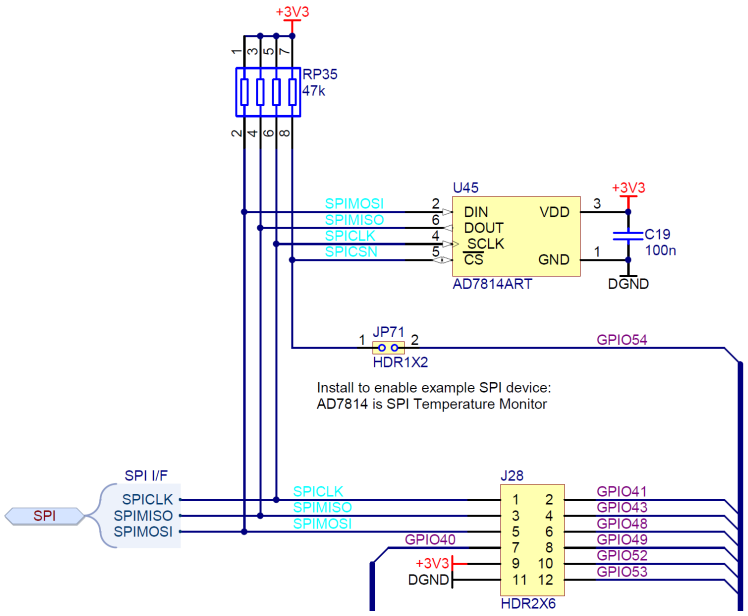

Figure 2-23: SPI Interface Configuration

3 SETTING UP AND USING THE BOARD

The default status of the Jumpers on the boards is as shown in Table 3-1.

For the meaning of the various jumpers, refer to Table 4-38 and RD 1.

Jumper	Jumper Setting	Comment
JP1	Installed 3-5 and 4-6	Connects TX0/RX0 to RS232 interface
JP2	Installed 3-5 and 4-6	Connects TX1/RX1 to RS232 interface
JP3-JP66	Installed 1-2 to connect all signals as GPIO	User sets these jumpers according to which configuration and interfaces are to be used. See section2.4.
JP67	No connections	Not normally used
JP68	Not defined	
JP69	Not defined	
JP70	Installed 1-2 and 3-4	10k pull ups enabled on I2C interface
JP71	Not installed	Install 1-2 to allow GPIO54 to act as SPI chip select of on-board SPI chip
JP72	Not installed	Only required for Direct Coupling
JP73	Not installed	Only required for Direct Coupling
JP74	Not installed	Only required for Direct Coupling
JP75	Not installed	Only required for Direct Coupling
JP76	Installed 1-2, 3-4, 5-6, 7-8	Only remove if on-board RAM and FLASH is to be disabled
JP77	Not installed	Only install if PROM writing is to be disabled
JP78	Installed 1-3	End-stub termination enabled – see section 2.5.1
JP79	Installed 1-3	End-stub termination enabled – see section 2.5.1
JP80	Installed 1-2	Can be used as current measure point for 3.3V supply to ASIC
JP81	Installed 1-2	Can be used as current measure point for 1.8V supply to ASIC
JP82	Not installed	Connections only required if External RESET switch is required.
JP83	Not installed	Prevents Watchdog time-out from resetting board. Install to allow Watchdog to reset board.
JP84	Installed 2-3	Uses Oscillator in socket X2 as main clock.
JP85	Not installed	Install to pull pin HIGH to enable PROM EDAC
JP86	Not installed	Connections only required if External DSU Break switch is required.
JP87	Not installed	Only install for internal PLL to be bypassed
JP88	Not installed	A separate 100 MHz osc.. is installed in X5 for SPW_CLK
JP89	Not used	Only used if a CPCI front panel would be installed.

Table 3-1: Default Status of Jumpers/Switches

To operate the unit stand alone on the bench top, connect the +5V power supply to the Power Socket J14 at the back of the unit.

The POWER LED should be illuminated indicating that the +3.3V power is active.

Upon power on, the Processor will start executing instructions beginning at the memory location 0x00000000, which is the start of the PROM. If the PROM is 'empty' or no valid program is installed, the first executed instruction will be invalid, and the processor will halt with an ERROR condition, with the ERROR LED illuminated.

To perform software download and debugging on the processor, a link from the Host computer to the DSU interface of the board is necessary. A connection to the DSU of the board can be made using a JTAG cable from the Host PC to the JTAG connector on the front of the PCB.

To perform program download and software debugging on the hardware it is necessary to use the Gaisler Research *GRMON* debugging software, installed on a host PC (as represented in Figure 2-15).

Note that it is necessary to use the 'PRO' version of GRMON, as the *GR712RC ASIC* incorporates FT features. It is not possible to use evaluation version of GRMON with this ASIC. Please refer to the *GRMON* documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

Starting *GRMON*, with the command:

grmon -ftdi -freq 48

will establish a link to the DSU, and will initialise the processor registers and timers.

In the example shown in Figure 3-1 a connection is being made with GRMON over the JTAG interface.

(Where '48' is is the clock frequency of the main processor oscillator).

Typing the command *flash* will reported the detected Flash Prom memory configuration and *info sys* will provide more information on the processors registers and internal cores as shown in Figure 3-3.

Program download and debugging can be performed in the usual manner. More information on the usage, commands and debugging features of *GRMON,* is given in the *GRMON Users Manual* and associated documentation.

```
richard@hp2510p:~$ sudo grmon/grmon.linux -ftdi -ramws 1 -u

 GRMON LEON debug monitor v1.1.44 professional version

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 For latest updates, go to http://www.gaisler.com/
 Comments or bug-reports to support@gaisler.com

 This debug version will expire on 1/8/2011
 JTAG chain: GR712RC

 Device ID: : 0x712
 GRLIB build version: 3696

 initialising ....................................
 detected frequency:  48 MHz

 Component                            Vendor
 LEON3FT SPARC V8 Processor           Gaisler Research
 LEON3FT SPARC V8 Processor           Gaisler Research
 AHB Debug JTAG TAP                   Gaisler Research
 GR Ethernet MAC                      Gaisler Research
 SatCAN controller                    Gaisler Research
 GRSPW2 Spacewire Link                Gaisler Research
 GRSPW2 Spacewire Link                Gaisler Research
 GRSPW2 Spacewire Link                Gaisler Research
 GRSPW2 Spacewire Link                Gaisler Research
 GRSPW2 Spacewire Link                Gaisler Research
 GRSPW2 Spacewire Link                Gaisler Research
 Actel MIL-STD-1553 BRM               Gaisler Research
 CCSDS Telecommand Decoder            Gaisler Research
 CCSDS Telemetry Encoder              Gaisler Research
 SLINK master                         Gaisler Research
 FT Memory Controller                 Gaisler Research
 AHB/APB Bridge                       Gaisler Research
 LEON3 Debug Support Unit             Gaisler Research
 AHB/APB Bridge                       Gaisler Research
 OC CAN controller                    Gaisler Research
 FT AHB static ram                    Gaisler Research
 Generic APB UART                     Gaisler Research
 Multi-processor Interrupt Ctrl       Gaisler Research
 Modular Timer Unit                   Gaisler Research
 SPI Controller                       Gaisler Research
 CAN bus multiplexer                  Gaisler Research
 General purpose registers            Gaisler Research
 ASCS Master                          Gaisler Research
 General purpose I/O port             Gaisler Research
 General purpose I/O port             Gaisler Research
 AMBA Wrapper for OC I2C-master       Gaisler Research
 Clock gating unit                    Gaisler Research
 AHB status register                  Gaisler Research
 Generic APB UART                     Gaisler Research
 Generic APB UART                     Gaisler Research
 Generic APB UART                     Gaisler Research
 Generic APB UART                     Gaisler Research
 Generic APB UART                     Gaisler Research
 Modular Timer Unit                   Gaisler Research

 Use command 'info sys' to print a detailed report of attached cores
grlib> flash

 Intel-style 8-bit flash on D[31:24]

 Manuf.    Intel
 Device    MT28F640J3

 Device ID 0adcffffc6019e49
 User   ID ffffffffffffffff
 1 x 8 Mbyte = 8 Mbyte total @ 0x00000000

CFI info
 flash family  : 1
 flash size    : 64 Mbit
 erase regions : 1
 erase blocks  : 64
```

Figure 3-1: GRMON Listing - 1

```
 write buffer  : 32 bytes
 region  0     : 64 blocks of 128 Kbytes

grlib> info sys
00.01:053   Gaisler Research  LEON3FT SPARC V8 Processor (ver 0x0)
             ahb master 0
01.01:053   Gaisler Research  LEON3FT SPARC V8 Processor (ver 0x0)
             ahb master 1
02.01:01c   Gaisler Research  AHB Debug JTAG TAP (ver 0x0)
             ahb master 2
03.01:01d   Gaisler Research  GR Ethernet MAC (ver 0x0)
             ahb master 3, irq 14
             apb: 80000e00 - 80000f00
04.01:080   Gaisler Research  SatCAN controller (ver 0x0)
             ahb master 4, irq 14
             ahb: fff20000 - fff20100
05.01:029   Gaisler Research  GRSPW2 Spacewire Link (ver 0x0)
             ahb master 5, irq 22
             apb: 80100800 - 80100900
06.01:029   Gaisler Research  GRSPW2 Spacewire Link (ver 0x0)
             ahb master 6, irq 23
             apb: 80100900 - 80100a00
07.01:029   Gaisler Research  GRSPW2 Spacewire Link (ver 0x0)
             ahb master 7, irq 24
             apb: 80100a00 - 80100b00
08.01:029   Gaisler Research  GRSPW2 Spacewire Link (ver 0x0)
             ahb master 8, irq 25
             apb: 80100b00 - 80100c00
09.01:029   Gaisler Research  GRSPW2 Spacewire Link (ver 0x0)
             ahb master 9, irq 26
             apb: 80100c00 - 80100d00
0a.01:029   Gaisler Research  GRSPW2 Spacewire Link (ver 0x0)
             ahb master 10, irq 27
             apb: 80100d00 - 80100e00
0b.01:072   Gaisler Research  Actel MIL-STD-1553 BRM (ver 0x0)
             ahb master 11, irq 14
             ahb: fff00000 - fff01000
0c.01:031   Gaisler Research  CCSDS Telecommand Decoder (ver 0x2)
             ahb master 12, irq 14
             ahb: fff10000 - fff10100
0d.01:030   Gaisler Research  CCSDS Telemetry Encoder (ver 0x0)
             ahb master 13, irq 29
             apb: 80000b00 - 80000c00
0e.01:02f   Gaisler Research  SLINK master (ver 0x1)
             ahb master 14, irq 13
             apb: 80000800 - 80000900
00.01:054   Gaisler Research  FT Memory Controller (ver 0x1)
             ahb: 00000000 - 20000000
             ahb: 20000000 - 40000000
             ahb: 40000000 - 80000000
             apb: 80000000 - 80000100
             8-bit prom @ 0x00000000
             32-bit static ram: 1 * 8192 kbyte @ 0x40000000
01.01:006   Gaisler Research  AHB/APB Bridge (ver 0x0)
             ahb: 80000000 - 80100000
02.01:004   Gaisler Research  LEON3 Debug Support Unit (ver 0x1)
             ahb: 90000000 - a0000000
             AHB trace 256 lines, 32-bit bus, stack pointer 0x407ffff0
             CPU#0 win 8, hwbp 2, itrace 256, V8 mul/div, srmmu, lddel 1, GRFPU
                   icache 4 * 4 kbyte, 32 byte/line lru
                   dcache 4 * 4 kbyte, 16 byte/line lru
             CPU#1 win 8, hwbp 2, itrace 256, V8 mul/div, srmmu, lddel 1, GRFPU
                   icache 4 * 4 kbyte, 32 byte/line lru
                   dcache 4 * 4 kbyte, 16 byte/line lru
03.01:006   Gaisler Research  AHB/APB Bridge (ver 0x0)
             ahb: 80100000 - 80200000
06.01:019   Gaisler Research  OC CAN controller (ver 0x1)
             irq 5
             ahb: fff30000 - fff31000
             cores: 2
07.01:050   Gaisler Research  FT AHB static ram (ver 0x12)
             ahb: a0000000 - a0100000
             apb: 80100000 - 80100100
             256 kbyte AHB ram @ 0xa0000000
```

Figure 3-2: GRMON Listing - 2

```
01.01:00c   Gaisler Research  Generic APB UART (ver 0x1)
             irq 2
             apb: 80000100 - 80000200
             baud rate 38461, DSU mode (FIFO debug)
02.01:00d   Gaisler Research  Multi-processor Interrupt Ctrl (ver 0x3)
             apb: 80000200 - 80000300
03.01:011   Gaisler Research  Modular Timer Unit (ver 0x0)
             irq 8
             apb: 80000300 - 80000400
             16-bit scaler, 4 * 32-bit timers, divisor 48
04.01:02d   Gaisler Research  SPI Controller (ver 0x2)
             irq 13
             apb: 80000400 - 80000500
             FIFO depth: 16, no slave select lines
             Maximum word length: 32 bits
05.01:081   Gaisler Research  CAN bus multiplexer (ver 0x0)
             apb: 80000500 - 80000600
06.01:087   Gaisler Research  General purpose registers (ver 0x0)
             apb: 80000600 - 80000700
07.01:043   Gaisler Research  ASCS Master (ver 0x0)
             irq 16
             apb: 80000700 - 80000800
             2 slaves, 16 bit words
09.01:01a   Gaisler Research  General purpose I/O port (ver 0x0)
             apb: 80000900 - 80000a00
0a.01:01a   Gaisler Research  General purpose I/O port (ver 0x0)
             apb: 80000a00 - 80000b00
0c.01:028   Gaisler Research  AMBA Wrapper for OC I2C-master (ver 0x1)
             irq 28
             apb: 80000c00 - 80000d00
0d.01:02c   Gaisler Research  Clock gating unit (ver 0x0)
             apb: 80000d00 - 80000e00
             GRMON did NOT enable clocks during initialization
0f.01:052   Gaisler Research  AHB status register (ver 0x0)
             irq 1
             apb: 80000f00 - 80001000
01.01:00c   Gaisler Research  Generic APB UART (ver 0x1)
             irq 17
             apb: 80100100 - 80100200
             baud rate 38461
02.01:00c   Gaisler Research  Generic APB UART (ver 0x1)
             irq 18
             apb: 80100200 - 80100300
             baud rate 38461
03.01:00c   Gaisler Research  Generic APB UART (ver 0x1)
             irq 19
             apb: 80100300 - 80100400
             baud rate 38461
04.01:00c   Gaisler Research  Generic APB UART (ver 0x1)
             irq 20
             apb: 80100400 - 80100500
             baud rate 38461
05.01:00c   Gaisler Research  Generic APB UART (ver 0x1)
             irq 21
             apb: 80100500 - 80100600
             baud rate 38461
06.01:038   Gaisler Research  Modular Timer Unit (ver 0x1)
             irq 7
             apb: 80100600 - 80100700
             8-bit scaler, 2 * 32-bit timers, divisor 48
grlib> lo Desktop/gr-test/leon3/samples/stanford
section: .text at 0x40000000, size 54288 bytes
section: .data at 0x4000d410, size 2080 bytes
total size: 56368 bytes (762.6 kbit/s)
read 278 symbols
entry point: 0x40000000
grlib> run
Starting
    Perm  Towers  Queens   Intmm      Mm  Puzzle   Quick  Bubble    Tree     FFT
      50      50      17      66     850     183      33      50     217     867

Nonfloating point composite is        111

Floating point composite is        744

Program exited normally.
grlib>
```

Figure 3-3: GRMON Listing - 3

4 INTERFACES AND CONFIGURATION

4.1 List of Front/Back Panel Connectors

Name	Function	Type	Description
J1A upper	UART-0	D9-S (Female)	Connections for Serial UART-10 (RS232)
J1B lower	UART-1	D9-S (Female)	Connections for Serial UART-1 (RS232)
J2A upper	CANBUS-0	Dual D9-P (male)	Connections for CANBUS-0 interface
J2B lower	CANBUS-1	Dual D9-P (male)	Connections for CANBUS-1 interface
J3	SPW-0	MDM9-S (female)	LVDS connections for Spacewire Interface-0
J4	SPW-1	MDM9-S (female)	LVDS connections for Spacewire Interface-1
J5	SPW-2	MDM9-S (female)	LVDS connections for Spacewire Interface-2
J6	SPW-3	MDM9-S (female)	LVDS connections for Spacewire Interface-3
J7	SPW-4	MDM9-S (female)	LVDS connections for Spacewire Interface-4
J8	SPW-5	MDM9-S (female)	LVDS connections for Spacewire Interface-5
J9	MEM I/O	AMP 5177984-5	Memory I/O connector -120 pin 0.8mm pitch
J10	ETHERNET	RJ45	10/100Mbit/s Ethernet Connector
J11	GEN I/O	AMP 5177984-2	General I/O connector – 80 pin 0.8mm pitch
J12	JTAG	USB-Mini-AB	JTAG signal interface (over USB)
J13	MIL-STD-1553	D9-P (male)	Dual MIL-STD-1553 interface
J14	POWER-IN	2.1mm center +ve	+5V DC power input connector
J15	SODIMM	144 pin SODIMM	Socket for SODIMM SDRAM module
J16	TX[9..0]	20 pin 0.1” Header	Pin connections for RS422 TX pairs 0 to 9
J17	TX[19..10]	20 pin 0.1” Header	Pin connections for RS422 TX pairs 10 to 19
J18	RX[9..0]	20 pin 0.1” Header	Pin connections for RS422 RX pairs 0 to 9
J19	RX[19..10]	20 pin 0.1” Header	Pin connections for RS422 RX pairs 10 to 19
J20	RX[27..20]	20 pin 0.1” Header	Pin connections for RS422 RX pairs 20 to 29
J21	GPIO[9..0]	20 pin 0.1” Header	Pin connections for PIO signals 0 to 9
J22	GPIO[19..10]	20 pin 0.1” Header	Pin connections for PIO signals 10 to 19
J23	GPIO[29..20]	20 pin 0.1” Header	Pin connections for PIO signals 20 to 29
J24	GPIO[39..30]	20 pin 0.1” Header	Pin connections for PIO signals 30 to 39
J25	GPIO[49..40]	20 pin 0.1” Header	Pin connections for PIO signals 40 to 49
J26	GPIO[59..50]	20 pin 0.1” Header	Pin connections for PIO signals 50 to 59
J27	GPIO[66..60]	20 pin 0.1” Header	Pin connections for PIO signals 60 to 66
J28	I2C-USER	12 pin 0.1” Header	Pin connections for User I2C interface
J29	SPI-USER	4 pin 0.1” Header	Pin connections for User SPI interface
J30	POWER-IN'	Mate-N-Lok 4pin	Alternative power input for 4 pin IDE style connector
J31	SPW_CLK	SMA	SPW Clock Monitor or Injection

Table 4-1: List of Connectors

Pin	Name	Comment
1		No connect
6		No connect
2	TXD-0	Transmit pin
7		No connect
3	RXD-0	Receive pin
8		No connect
4		No connect
9		No connect
5	GND	Ground

Table 4-2: J1A (upper connector) UART-0 - Serial Interface (RS232) connections

Pin	Name	Comment
1		No connect
6		No connect
2	TXD-1	Transmit pin
7		No connect
3	RXD-1	Receive pin
8		No connect
4		No connect
9		No connect
5	GND	Ground

Table 4-3: J1B (lower connector) UART-1 - Serial Interface (RS232) connections

Pin	Name	Comment
1		No connect
6	GND	Ground
2	CAN1_L	CAN Dominant Low
7	CAN1_H	CAN Dominant High
3	GND	Ground
8		No connect
4		No connect
9		No connect
5	CANSHD1	Shield

Table 4-4: J2A (upper connector) CANBUS-1 interface connections

Pin	Name	Comment
1		No connect
6	DGND	Ground
2	CAN0_L	CAN Dominant Low
7	CAN0_H	CAN Dominant High
3	DGND	Ground
8		No connect
4		No connect
9		No connect
5	CANSHD0	Shield

Table 4-5: J2B (lower connector) CANBUS-0 interface connections

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 4-6: J3 SPW-0 interface connections

Pin	Name	Comment
1	DIN1+	Data In +ve
6	DIN1-	Data In -ve
2	SIN1+	Strobe In +ve
7	SIN1-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT1+	Strobe Out +ve
4	SOUT1-	Strobe Out -ve
9	DOUT1+	Data Out +ve
5	DOUT1-	Data Out -ve

Table 4-7: J4 SPW-1 interface connections

Pin	Name	Comment
1	DIN2+	Data In +ve
6	DIN2-	Data In -ve
2	SIN2+	Strobe In +ve
7	SIN2-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT2+	Strobe Out +ve
4	SOUT2-	Strobe Out -ve
9	DOUT2+	Data Out +ve
5	DOUT2-	Data Out -ve

Table 4-8: J5 SPW-2 interface connections

Pin	Name	Comment
1	DIN3+	Data In +ve
6	DIN3-	Data In -ve
2	SIN3+	Strobe In +ve
7	SIN3-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT3+	Strobe Out +ve
4	SOUT3-	Strobe Out -ve
9	DOUT3+	Data Out +ve
5	DOUT3-	Data Out -ve

Table 4-9: J6 SPW-3 interface connections

Pin	Name	Comment
1	DIN2+	Data In +ve
6	DIN4-	Data In -ve
2	SIN4+	Strobe In +ve
7	SIN4-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT4+	Strobe Out +ve
4	SOUT4-	Strobe Out -ve
9	DOUT4+	Data Out +ve
5	DOUT4-	Data Out -ve

Table 4-10: J7 SPW-4 interface connections

Pin	Name	Comment
1	DIN5+	Data In +ve
6	DIN5-	Data In -ve
2	SIN5+	Strobe In +ve
7	SIN5-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT5+	Strobe Out +ve
4	SOUT5-	Strobe Out -ve
9	DOUT5+	Data Out +ve
5	DOUT5-	Data Out -ve

Table 4-11: J8 SPW-5 interface connections

FUNCTION	ASIC pin	CONNECTOR PIN		ASIC pin	FUNCTION
DGND		1	120		DGND
+5V		2	119		+5V
DGND		3	118		DGND
-12V		4	117		-12V
DGND		5	116		DGND
+12V		6	115		+12V
DGND		7	114		DGND
D15	40	8	113	16	D31
D7	52	9	112	26	D23
+3.3V		10	111		+3.3V
DGND		11	110		DGND
D14	41	12	109		D30
D6	53	13	108	27	D22
D13	42	14	107	20	D29
D5	54	15	106	32	D21
D12	43	16	105	21	D28
D4	55	17	104	33	D20
D11	44	18	103	22	D27
D3	56	19	102	34	D19
+3.3V		20	101		+3.3V
DGND		21	100		DGND
D10	45	22	99		D26
D2	57	23	98	35	D18
D9	46	24	97	24	D25
D1	58	25	96	36	D17
D8	49	26	95	25	D24
D0	59	27	94	37	D16
(DGND)		28	93		(DGND)
(DGND)		29	92		(DGND)
+3.3V		30	91		+3.3V
DGND		31	90		DGND
A22	87	32	89	85	A23
A20	92	33	88	88	A21
A18	97	34	87	95	A19
A16	98	35	86	99	A17
A14	89	36	85	96	A15
A12	82	37	84	86	A13
A10	80	38	83	81	A11
A8	74	39	82	77	A9
+3.3V		40	81		+3.3V
DGND		41	80		DGND
A6	72	42	79	73	A7
A4	68	43	78	71	A5
A2	64	44	77	65	A3
A0	62	45	76	63	A1
WRITEN	107	46	75	120	READ
OEN	126	47	74	108	IOSN
ROMSN0	101	48	73		ROMSN1
(+3.3V)		49	72		(+3.3V)
+3.3V		50	71		+3.3V
DGND		51	70		DGND
(+3.3V)		52	69	111	RAMOEN
(+3.3V)		53	68	111	RAMOEN
RAMSN1	110	54	67	111	RAMOEN
RAMSN0	109	55	66	111	RAMOEN
RWEN	112	56	65	112	RWEN
RWEN	112	57	64	112	RWEN
BRDYN	113	58	63	118	BEXCN
RESETN		59	62		CLK
DGND		60	61		DGND

Table 4-12: Expansion connector J9 Pin-out (see also section 2.3.4)

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 4-13: J10 RJ45-ETHERNET Connector

FUNCTION	ASIC pin	CONNECTOR PIN			FUNCTION
DGND		1	60		DGND
CB6	5	2	59	141	CB7
CB4	9	3	58	8	CB5
CB2	11	4	57	10	CB3
CB0	15	5	56	12	CB1
		6	55		
		7	54		
		8	53		
		9	52		
DGND		10	51		DGND
+3.3V		11	50		+3.3V
		12	49		
		13	48		
		14	47		
		15	46		
		16	45		
		17	44		
		18	43		
		19	42		
DGND		20	41		DGND
+3.3V		21	40		+3.3V
		22	39		
		23	38		
		24	37		
		25	36		
		26	35		
		27	34		
		28	33		
		29	32		
DGND		30	31		DGND

Table 4-14: Expansion connector J11 Pin-out (see also section 2.3.4)

Pin	Name	Comment
1	VDD	+5V (from external device)
2	DM	Data Minus
3	DP	Data Plus
4	DGND	Ground

Table 4-15: J12 ASIC– JTAG Connector (over USB)

Pin	Name	Comment
1	BUS_0	BUS_0 positive
6	GND	Ground
2	BUS_0B	BUS_0 negative
7		No connect
3		No connect
8		No connect
4	BUS_1	BUS_1 positive
9	GND	Ground
5	BUS_1B	BUS_1 negative

Table 4-16: J13 Dual MIL-STD-1553 interface connections

Pin	Name	Comment
+VE	+5V	Inner Pin, 5V, typically TBD A
-VE	GND	Outer Pin Return

Table 4-17: J14 POWER – External Power Connector

FUNCTION	ASIC PIN	CONNECTOR PIN		ASIC PIN	FUNCTION
DGND		1	2		DGND
D31		3	4		CB7
D30		5	6		CB6
D29		7	8		CB5
D28		9	10		CB4
+3.3V		11	12		+3.3V
D27		13	14		CB3
D26		15	16		CB2
D25		17	18		CB1
D24		19	20		CB0
DGND		21	22		DGND
SDDQM3		23	24		SDDQM0
SDDQM2		25	26		SDDQM5 / pulled high
+3.3V		27	28		+3.3V
A2		29	30		A5
A3		31	32		A6
A4		33	34		A7
DGND		35	36		DGND
D23		37	38		nc
D22		39	40		nc
D21		41	42		nc
D20		43	44		nc
+3.3V		45	46		+3.3V
D19		47	48		nc
D18		49	50		nc
D17		51	52		nc
D16		53	54		nc
DGND		55	56		DGND
nc		57	58		nc
nc		59	60		nc
SDCLK0		61	62		SDCKE0/ pulled high
+3.3V		63	64		+3.3V
SDRASN		65	66		SDCASN
SDWEN		67	68		SDCKE1/ pulled high
SDCSN0		69	70		A17
SDCSN1		71	72		A14
nc		73	74		SDCLK1
DGND		75	76		DGND
nc		77	78		nc
nc		79	80		nc
+3.3V		81	82		+3.3V
D15		83	84		nc
D14		85	86		nc
D13		87	88		nc
D12		89	90		nc
DGND		91	92		DGND
D11		93	94		nc
D10		95	96		nc
D9		97	98		nc
D8		99	100		nc
+3.3V		101	102		+3.3V
A8		103	104		A9
A10		105	106		A15 (SBA0)
DGND		107	108		DGND
A11		109	110		A16 (SBA1)
A12		111	112		A13
+3.3V		113	114		+3.3V
SDDQM1		115	116		SDDQM6 / pulled high
SDDQM0		117	118		SDDQM7 / pulled high
DGND		119	120		DGND
D7		121	122		nc
D6		123	124		nc
D5		125	126		nc
D4		127	128		nc
+3.3V		129	130		+3.3V
D3		131	132		nc
D2		133	134		nc
D1		135	136		nc
D0		137	138		nc
DGND		139	140		DGND
SDSDA / pulled high		141	142		SDSCL / pulled high
+3.3V		143	144		+3.3V

Table 4-18: SODIMM socket J15 Pin-out

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
TX0P		1	2	TX0N
TX1P		3	4	TX1N
TX2P		5	6	TX2N
TX3P		7	8	TX3N
TX4P		9	10	TX4N
TX5P		11	12	TX5N
TX6P		13	14	TX6N
TX7P		15	16	TX7N
TX8P		17	18	TX8N
TX9P		19	20	TX9N

Table 4-19: J16 RS422 Transmitter Pairs

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
TX10P		1	2	TX10N
TX11P		3	4	TX11N
TX12P		5	6	TX12N
TX13P		7	8	TX13N
TX14P		9	10	TX14N
TX15P		11	12	TX15N
TX16P		13	14	TX16N
TX17P		15	16	TX17N
TX18P		17	18	TX18N
TX19P		19	20	TX19N

Table 4-20: J17 RS422 Transmitter Pairs

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
RX0P		1	2	RX0N
RX1P		3	4	RX1N
RX2P		5	6	RX2N
RX3P		7	8	RX3N
RX4P		9	10	RX4N
RX5P		11	12	RX5N
RX6P		13	14	RX6N
RX7P		15	16	RX7N
RX8P		17	18	RX8N
RX9P		19	20	RX9N

Table 4-21: J18 RS422 Receiver Pairs

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
RX10P		1	2	RX10N
RX11P		3	4	RX11N
RX12P		5	6	RX12N
RX13P		7	8	RX13N
RX14P		9	10	RX14N
RX15P		11	12	RX15N
RX16P		13	14	RX16N
RX17P		15	16	RX17N
RX18P		17	18	RX18N
RX19P		19	20	RX19N

Table 4-22: J19 RS422 Receiver Pairs

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
RX20P		1	2	RX20N
RX21P		3	4	RX21N
RX22P		5	6	RX22N
RX23P		7	8	RX23N
RX24P		9	10	RX24N
RX25P		11	12	RX25N
RX26P		13	14	RX26N
RX27P		15	16	RX27N
nc		17	18	nc
nc		19	20	nc

Table 4-23: J20 RS422 Receiver Pairs

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
GPIO0		1	2	DGND
GPIO1		3	4	DGND
GPIO2		5	6	DGND
GPIO3		7	8	DGND
GPIO4		9	10	DGND
GPIO5		11	12	DGND
GPIO6		13	14	DGND
GPIO7		15	16	DGND
GPIO8		17	18	DGND
GPIO9		19	20	DGND

Table 4-24: J21 PIO Header Pin out

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
GPIO10		1	2	DGND
GPIO11		3	4	DGND
GPIO12		5	6	DGND
GPIO13		7	8	DGND
GPIO14		9	10	DGND
GPIO15		11	12	DGND
GPIO16		13	14	DGND
GPIO17		15	16	DGND
GPIO18		17	18	DGND
GPIO19		19	20	DGND

Table 4-25: J22 PIO Header Pin out

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
GPIO20		1	2	DGND
GPIO21		3	4	DGND
GPIO22		5	6	DGND
GPIO23		7	8	DGND
GPIO24		9	10	DGND
GPIO25		11	12	DGND
GPIO26		13	14	DGND
GPIO27		15	16	DGND
GPIO28		17	18	DGND
GPIO29		19	20	DGND

Table 4-26: J23 PIO Header Pin out

FUNCTION	ASIC pin	CONNECTOR PIN			FUNCTION
GPIO30		1	■	2	DGND
GPIO31		3	□	4	DGND
GPIO32		5	□	6	DGND
GPIO33		7	□	8	DGND
GPIO34		9	□	10	DGND
GPIO35		11	□	12	DGND
GPIO36		13	□	14	DGND
GPIO37		15	□	16	DGND
GPIO38		17	□	18	DGND
GPIO39		19	□	20	DGND

Table 4-27: J24 PIO Header Pin out

FUNCTION	ASIC pin	CONNECTOR PIN			FUNCTION
GPIO40		1	■	2	DGND
GPIO41		3	□	4	DGND
GPIO42		5	□	6	DGND
GPIO43		7	□	8	DGND
GPIO44		9	□	10	DGND
GPIO45		11	□	12	DGND
GPIO46		13	□	14	DGND
GPIO47		15	□	16	DGND
GPIO48		17	□	18	DGND
GPIO49		19	□	20	DGND

Table 4-28: J25 PIO Header Pin out

FUNCTION	ASIC pin	CONNECTOR PIN			FUNCTION
GPIO50		1	■	2	DGND
GPIO51		3	□	4	DGND
GPIO52		5	□	6	DGND
GPIO53		7	□	8	DGND
GPIO54		9	□	10	DGND
GPIO55		11	□	12	DGND
GPIO56		13	□	14	DGND
GPIO57		15	□	16	DGND
GPIO58		17	□	18	DGND
GPIO59		19	□	20	DGND

Table 4-29: J26 PIO Header Pin out

FUNCTION	ASIC pin	CONNECTOR PIN			FUNCTION
GPIO60		1	■	2	DGND
GPIO61		3	□	4	DGND
GPIO62		5	□	6	DGND
GPIO63		7	□	8	DGND
GPIO64		9	□	10	DGND
GPIO65		11	□	12	DGND
GPIO66		13	□	14	DGND
nc		15	□	16	DGND
nc		17	□	18	DGND
nc		19	□	20	DGND

Table 4-30: J27 PIO Header Pin out

Pin	Name	Comment
1	+5V	+5V, typically TBD A
2	GND	Ground
3	+12V	+12V Not used
4	GND	Ground

Table 4-31: J30 POWER – External Power Connector

Pin	Name	Comment
centre	SPWCLK	Clock
outer	GND	Ground

Table 4-32: J31 SPW Clock

4.2 List of Oscillators, Switches and LED's

Name	Function	Description
X1	OSC_MAIN	Oscillator for main ASIC clock, SMD type, 3.3V, 48MHz
X2	OSC_USER	Alternative User oscillator for main ASIC clock, DIL8 socket, 3.3V
X3	OSC_1553	Oscillator for 1553 interface functions , 24.0MHz
X4	OSC_ETH	Oscillator for Ethernet PHY transceiver, SMD type, 3.3V, 50.000MHz
X5	OSC_SPW	DIL8 socket for user installed SPW Clock Oscillator, 3.3V
Y1	XTAL_RTC	32.768kHz crystal for I2C Real Time Clock

Table 4-33: List and definition of Oscillators

Name	Function	Description
D1	POWER (3.3V)	Power indicator
D2	ERRORN	Leon processor in 'ERROR' mode
D3	PROM_BUSY	Prom Write/Erase in Progress
D4	WDOG	Watchdog indicator

Table 4-34: List and definition of PCB mounted LED's

Name	Function	Description
S1	RESET	Push button RESET switch
S2	Not used	Not used

Table 4-35: List and definition of Switches

4.3 List of Jumpers

Name	Function	Type	Description
JP1	SWMX0 & 1	2X3 pin 0.1” Header	Connects UART0 signals to RS422 or RS232 circuits
JP2	SWMX2	2X3 pin 0.1” Header	Connects UART1 signals to RS422 or RS232 circuits
JP3	SWMX3	2X6 2mm Header	Configuration jumper for SWMX3 pin
JP4	SWMX4	2X6 2mm Header	Configuration jumper for SWMX4 pin
JP5	SWMX5	2X6 2mm Header	Configuration jumper for SWMX5 pin
JP6	SWMX6	2X6 2mm Header	Configuration jumper for SWMX6 pin
JP7	SWMX7	2X6 2mm Header	Configuration jumper for SWMX7 pin
JP8	SWMX8	2X6 2mm Header	Configuration jumper for SWMX8 pin
JP9	SWMX9	2X6 2mm Header	Configuration jumper for SWMX9 pin
JP10	SWMX10	2X6 2mm Header	Configuration jumper for SWMX10 pin
JP11	SWMX11	2X6 2mm Header	Configuration jumper for SWMX11 pin
JP12	SWMX12	2X6 2mm Header	Configuration jumper for SWMX12 pin
JP13	SWMX13	2X6 2mm Header	Configuration jumper for SWMX13 pin
JP14	SWMX14	2X6 2mm Header	Configuration jumper for SWMX14 pin
JP15	SWMX15	2X6 2mm Header	Configuration jumper for SWMX15 pin
JP16	SWMX16	2X6 2mm Header	Configuration jumper for SWMX16 pin
JP17	SWMX17	2X6 2mm Header	Configuration jumper for SWMX17 pin
JP18	SWMX18	2X6 2mm Header	Configuration jumper for SWMX18 pin
JP19	SWMX19	2X6 2mm Header	Configuration jumper for SWMX19 pin
JP20	SWMX20	2X6 2mm Header	Configuration jumper for SWMX20 pin
JP21	SWMX21	2X6 2mm Header	Configuration jumper for SWMX21 pin
JP22	SWMX22	2X6 2mm Header	Configuration jumper for SWMX22 pin
JP23	SWMX23	2X6 2mm Header	Configuration jumper for SWMX23 pin
JP24	SWMX24	2X6 2mm Header	Configuration jumper for SWMX24 pin
JP25	SWMX25	2X6 2mm Header	Configuration jumper for SWMX25 pin
JP26	SWMX26	2X6 2mm Header	Configuration jumper for SWMX26 pin
JP27	SWMX27	2X6 2mm Header	Configuration jumper for SWMX27 pin
JP28	SWMX28	2X6 2mm Header	Configuration jumper for SWMX28 pin
JP29	SWMX29	2X6 2mm Header	Configuration jumper for SWMX29 pin
JP30	SWMX30	2X6 2mm Header	Configuration jumper for SWMX30 pin
JP31	SWMX31	2X6 2mm Header	Configuration jumper for SWMX31 pin
JP32	SWMX32	2X6 2mm Header	Configuration jumper for SWMX32 pin
JP33	SWMX33	2X6 2mm Header	Configuration jumper for SWMX33 pin
JP34	SWMX34	2X6 2mm Header	Configuration jumper for SWMX34 pin
JP35	SWMX35	2X6 2mm Header	Configuration jumper for SWMX35 pin

Table 4-36: List and definition of PCB Jumpers, part 1

(for details refer to schematic, RD 1)

Name	Function	Type	Description
JP36	SWMX36	2X6 2mm Header	Configuration jumper for SWMX36 pin
JP37	SWMX37	2X6 2mm Header	Configuration jumper for SWMX37 pin
JP38	SWMX38	2X6 2mm Header	Configuration jumper for SWMX38 pin
JP39	SWMX39	2X6 2mm Header	Configuration jumper for SWMX39 pin
JP40	SWMX40	2X6 2mm Header	Configuration jumper for SWMX40 pin
JP41	SWMX41	2X6 2mm Header	Configuration jumper for SWMX41 pin
JP42	SWMX42	2X6 2mm Header	Configuration jumper for SWMX42 pin
JP43	SWMX43	2X6 2mm Header	Configuration jumper for SWMX43 pin
JP44	SWMX44	2X6 2mm Header	Configuration jumper for SWMX44 pin
JP45	SWMX45	2X6 2mm Header	Configuration jumper for SWMX45 pin
JP46	SWMX46	2X6 2mm Header	Configuration jumper for SWMX46 pin
JP47	SWMX47	2X6 2mm Header	Configuration jumper for SWMX47 pin
JP48	SWMX48	2X6 2mm Header	Configuration jumper for SWMX48 pin
JP49	SWMX49	2X6 2mm Header	Configuration jumper for SWMX49 pin
JP50	SWMX50	2X6 2mm Header	Configuration jumper for SWMX50 pin
JP51	SWMX51	2X6 2mm Header	Configuration jumper for SWMX51 pin
JP52	SWMX52	2X6 2mm Header	Configuration jumper for SWMX52 pin
JP53	SWMX53	2X6 2mm Header	Configuration jumper for SWMX53 pin
JP54	SWMX54	2X6 2mm Header	Configuration jumper for SWMX54 pin
JP55	SWMX55	2X6 2mm Header	Configuration jumper for SWMX55 pin
JP56	SWMX56	2X6 2mm Header	Configuration jumper for SWMX56 pin
JP57	SWMX57	2X6 2mm Header	Configuration jumper for SWMX57 pin
JP58	SWMX58	2X6 2mm Header	Configuration jumper for SWMX58 pin
JP59	SWMX59	2X6 2mm Header	Configuration jumper for SWMX59 pin
JP60	SWMX60	2X6 2mm Header	Configuration jumper for SWMX60 pin
JP61	SWMX61	2X6 2mm Header	Configuration jumper for SWMX61 pin
JP62	SWMX62	2X6 2mm Header	Configuration jumper for SWMX62 pin
JP63	SWMX63	2X6 2mm Header	Configuration jumper for SWMX63 pin
JP64	SWMX64	2X6 2mm Header	Configuration jumper for SWMX64 pin
JP65	SWMX65	2X6 2mm Header	Configuration jumper for SWMX65 pin
JP66	SWMX66	2X6 2mm Header	Configuration jumper for SWMX66 pin
JP67	SPARE RS422	4 pin 0.1” Header	Header providing access to Spare RS422 signals
JP68	---	---	Not used
JP69	---	---	Not used
JP70	I2C-PULLUP	2X2 pin 0.1” Header	Install pull ups on I2C signals
JP71	SPI_CSN	1X2 pin 0.1” Header	Enable/Disable on board SPI circuit

Table 4-37: List and definition of PCB Jumpers, part 2

(for details refer to schematic, RD 1)

Name	Function	Type	Description
JP72	BUS0	1X2 pin 0.1” Header	Install for MIL-STD-1553A direct coupling
JP73	BUS0B	1X2 pin 0.1” Header	Install for MIL-STD-1553A direct coupling
JP74	BUS1	1X2 pin 0.1” Header	Install for MIL-STD-1553A direct coupling
JP75	BUS1B	1X2 pin 0.1” Header	Install for MIL-STD-1553A direct coupling
JP76	RAM_BANK	4x2 pin 0.1” Header	Header for configuration of ROM/RAM bank select
JP77	PROM_WR	1X2 pin 0.1” Header	Install to Disable PROM writing
JP78	CAN_TERM0	2x2 pin 0.1” Header	Header for configuration of Termination of CAN0 i/f
JP79	CAN_TERM1	2x2 pin 0.1” Header	Header for configuration of Termination of CAN1 i/f
JP80	I3V3	2 pin 0.1” Header	Measure point for 3.3V current (Link normally installed)
JP81	I1V8	2 pin 0.1” Header	Measure point for 1.8V current (Link normally installed)
JP82	JP_RESET	1X2 pin 0.1” Header	Pins for external RESET switch
JP83	WD_EN	1X2 pin 0.1” Header	Jumper to enable Watchdog to cause board reset
JP84	CLK_CONFIG	1X3 pin 0.1” Header	Connects either X1 to X2 oscillator to Main oscillator
JP85	PROM_EDAC	1X2 pin 0.1” Header	Install to pull pin HIGH to enable PROM EDAC
JP86	JP_BREAK	1X2 pin 0.1” Header	Pins for external BREAK switch
JP87	DLL_BP	1X2 pin 0.1” Header	Install jumper to Bypass internal PLL circuit
JP88	SPW_OSC	1X2 pin 0.1” Header	Connects MAIN_CLK also as SPW_CLK
JP89	FP_LEDS	4x2 pin 0.1” Header	Header to connect to front panel LED's

Table 4-38: List and definition of PCB Jumpers, part 3

(for details refer to schematic, RD 1)

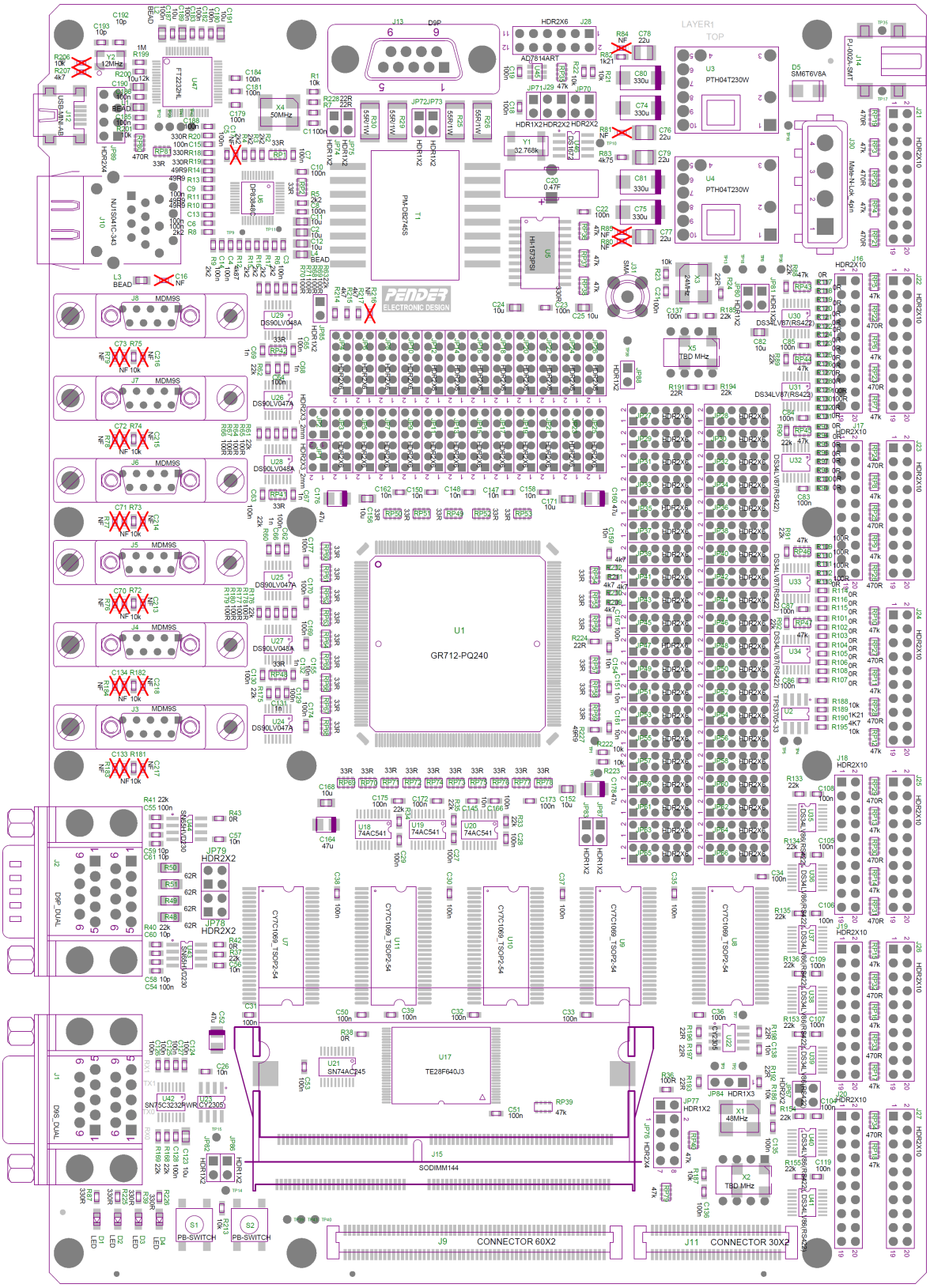

Figure 4-2: PCB Top Assembly View

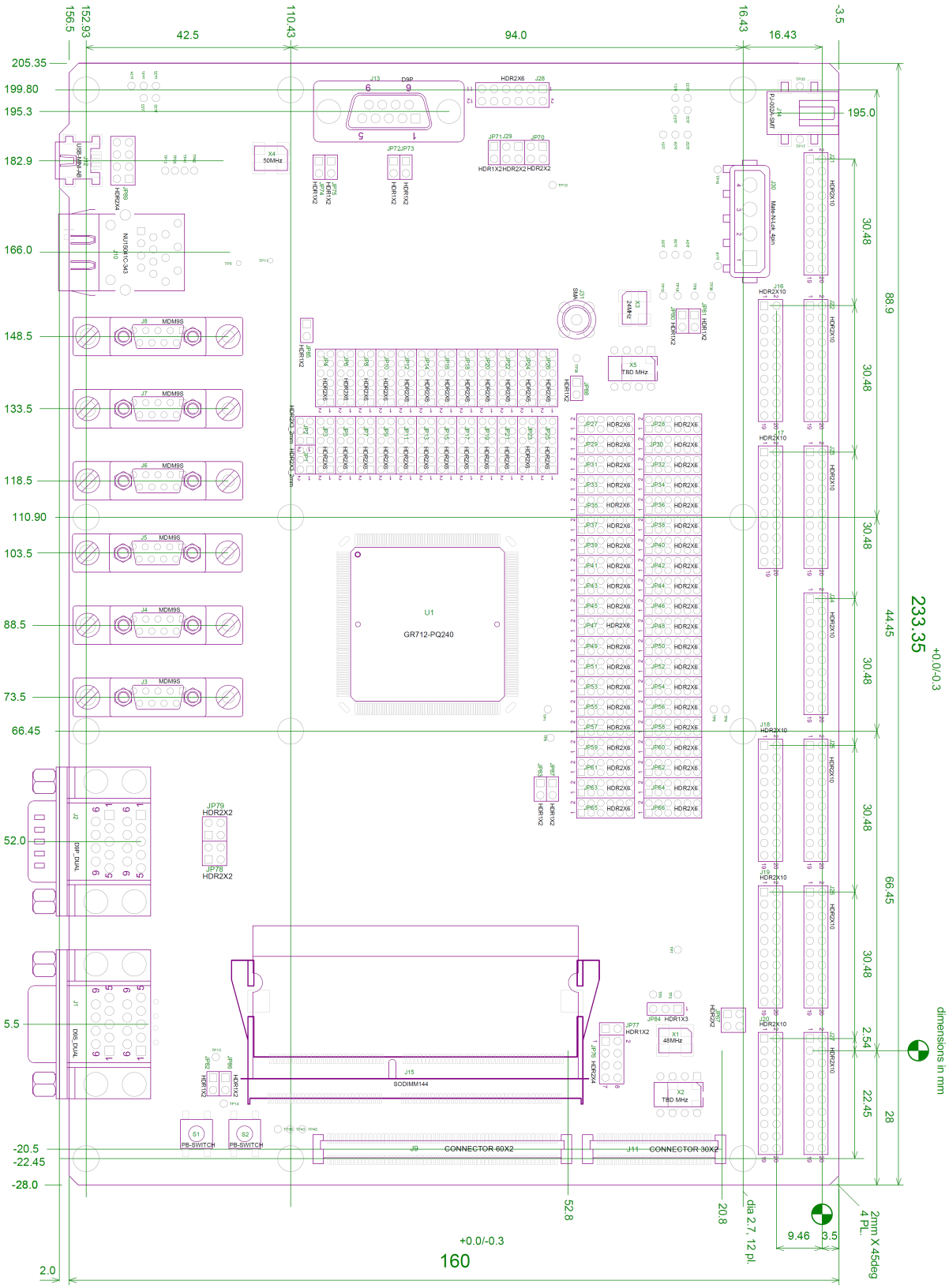

Figure 4-3: PCB Connector Positions

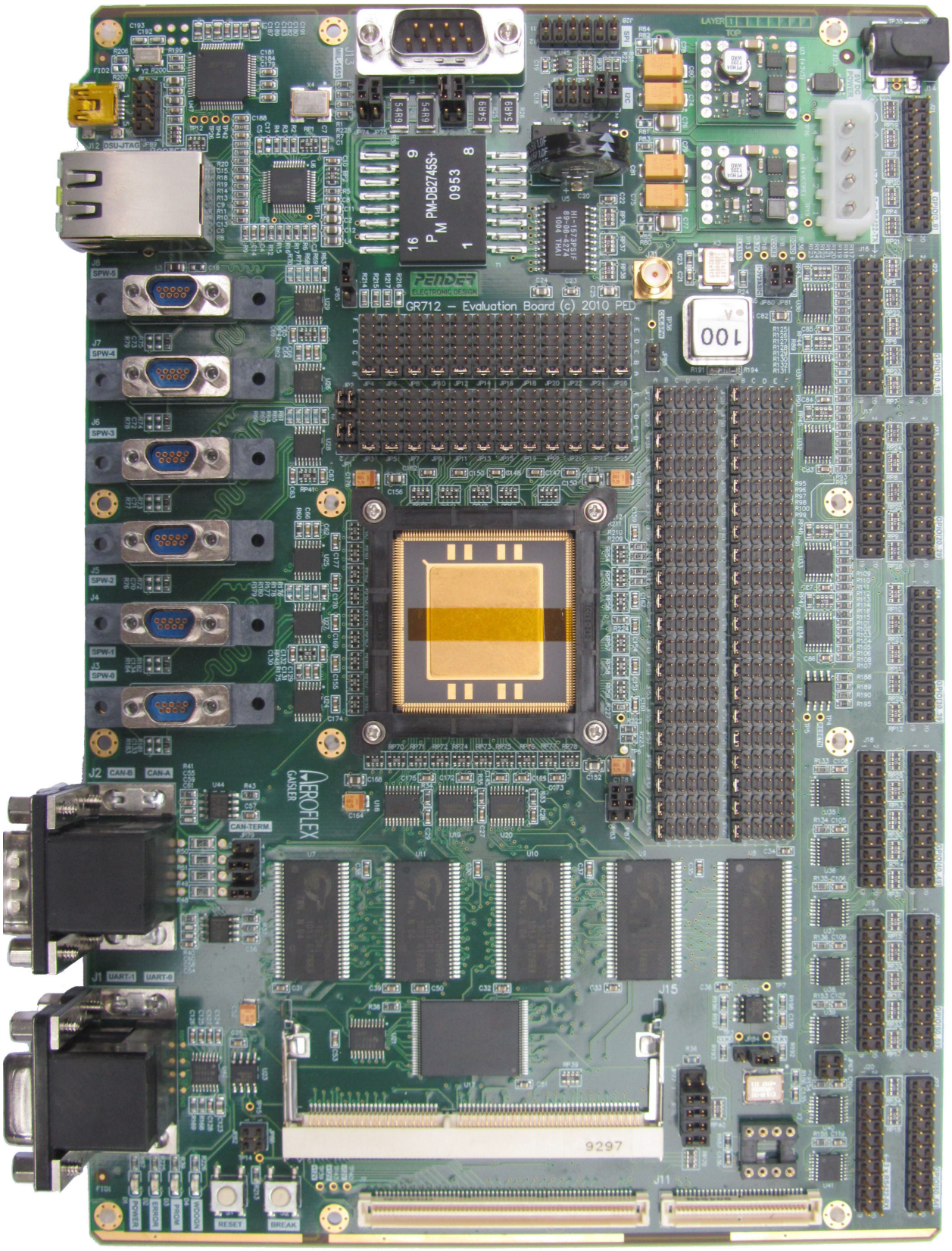

Figure 4-4: GR712 Assembly Photo